

EXHIBIT D

**UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

PHENIX LONGHORN LLC,

Plaintiff,

v.

INNOLUX CORPORATION,

Defendant.

§
§
§
§
§
§
§
§
§
§
§

Civil Action No. 2:23-cv-478

JURY TRIAL DEMANDED

DECLARATION OF PAUL S. MIN, PH.D.
REGARDING CLAIM CONSTRUCTION FOR
U.S. PATENT NOS. 7,233,305 AND 7,557,788

I, Paul S. Min, Ph.D., declare:

I. Qualifications and Background Information

1. My name is Paul S. Min. I have been retained in this litigation on behalf of Defendant Innolux Corporation (“Defendant” or “Innolux”).

2. I reside in St. Louis, Missouri, where I am employed by the Washington University in St. Louis.

3. I understand that Phenix Longhorn, LLC (“Phenix” or “Plaintiff”) has claimed that Innolux is infringing certain claims of U.S. Patent 7,233,305 (the “‘305 Patent”) and U.S. Patent 7,557,788 (the “‘788 Patent”) (collectively, the “Asserted Patents”). Specifically, I understand that Phenix has asserted claims 1, 2, and 5 of the ‘305 Patent and claim 1 of the ‘788 Patent.

4. I have been asked to provide expert testimony in this litigation regarding the understanding of a person of ordinary skill in the art (“POSA”) of the Asserted Patents at the time of the invention and the meaning of certain claim terms and limitations within the Asserted Claims. I am over eighteen years of age, and I am competent to testify regarding the matters set forth in this Declaration if I am called upon to do so. This Declaration includes the opinions I would offer if called to do so at a claim construction hearing. I reserve the right to provide further opinions in this case, such as opinions regarding non-infringement or invalidity of the Asserted Patents, if requested at a later time. I further reserve the right to respond to any opinions presented by experts retained by Phenix regarding the meaning of any claim term or limitation within the Asserted Claims.

5. The opinions I provide in this expert Declaration are my own and are based on my analysis in this matter and on the knowledge, education, experience, training, and skill I have accumulated in the course of my over 40-year career in computers and electronics. They also are based on certain legal principles provided to me by counsel for Innolux, which are identified in this Declaration. My opinions are also based on the information I considered in connection with the preparation of this Declaration. This information includes, but is not limited to, the Asserted Patents, their file histories, the parties’ identification and proposed claim constructions for the various disputed terms of the Asserted Claims, and the references cited in support of the parties’ constructions. Between now and when I may be asked to testify or be deposed on my opinions relating to claim construction, I expect to continue my review, evaluation, and analysis of information generated during the discovery process.

A. Compensation

6. Innolux is paying my customary rate of \$500 per hour for my time spent in study, preparation, and testifying in this case. I am also being reimbursed for reasonable and customary expenses associated with my work in this case. No portion of my compensation is dependent or otherwise contingent upon the specifics of my testimony or the results of this lawsuit.

B. Educational Background and Career History

7. I received a Bachelor of Science degree in Electrical Engineering in 1982, a Master of Science degree in Electrical Engineering in 1984, and a Ph.D. in Electrical Engineering in 1987, all from The University of Michigan in Ann Arbor. Currently, I am a Senior Professor in the Department of Electrical and Systems Engineering at Washington University in St. Louis, a position I have held since 2015, and I have been with the university since 1990. A current copy of my curriculum vitae is attached as **Exhibit A**.

8. After receiving my Ph.D., I was a Member of Technical Staff in the New Network Architecture Development Group at Bellcore in New Jersey from September 1987 to August 1990. Following my time at Bellcore, I joined Washington University in St. Louis as an Assistant Professor in the Department of Electrical Engineering in 1990 and was later promoted to Associate Professor with tenure in 1996. From 1997 to 1999, I additionally founded and served as President of MinMax Technologies, Inc., a fabless semiconductor company focused on designing high-performance switching ASICs. Subsequently, I founded Erlang Technology, Inc. in St. Louis, Missouri, and served as its President from 1999 to 2008. Erlang Technology, which focused on high-speed packet switching and related technologies, raised \$40M in total capital and received a “Product of the Year” Award from Analog Zone Magazine in 2004.

9. I am listed as an inventor on multiple U.S. patents, including those related to network devices, hierarchical pattern matching, WFQ scheduling, high-speed packet switching, multi-dimensional index trees, and multi-channel switching. I have authored or co-authored numerous publications and conference presentations in areas such as wireless sensor networks, cloud computing, network switching and routing, and mobile application virtualization. My curriculum vitae lists these patents and publications. I have held various leadership positions within the St. Louis Section of the Institute of Electrical and Electronics Engineers (IEEE), including Chair.

10. I have worked in the fields of electrical engineering, computer communications, network systems, and semiconductor design for over three decades. I taught the information theory at graduate level including the gamma encoding. Moreover, I have extensive background in designing and development of controllers for the semiconductor devices. In early 2000s, I have consulted with the LG Philips Display, a Korean company, in their manufacturing of LCD and plasma panels, which included panel testing.

11. My career has spanned academia and industry, involving research, teaching, and the development and commercialization of advanced technologies.

12. During the last ten years, I have provided testimony as an expert witness in the following cases:

- *Certain Audio Players and Components thereof (II)*, Inv. No. 337-TA-1330 (U.S.I.T.C. June 2023) (Testifying Expert for Google Inc.)
- *Atlas Global Technologies LLC v. ASUSTek Computers Inc.*, No. 6:21-cv-820 (W.D. Tex. Nov. 2023) (Testifying Expert for ASUSTek)
- *Bell N. Research, LLC v. HMD Am., Inc.*, No. 1:22-cv-22706-SCOLA/GOODMAN (S.D. Fla. Dec. 2023) (Testifying Expert for HMD)

- *Atlas Global Technologies LLC v. ZyXEL Commc'ns Corp.*, No. 6:22-cv-00355 (W.D. Tex. Ret. Mar. 2023) (Testifying Expert for ZyXel)
- *Atlas Global Technologies LLC v. D-Link Corp.*, No. 6:22-cv-00520 (W.D. Tex. Ret. Mar. 2023) (Testifying Expert for ZyXel)
- *Bell N. Research v. MediaTek Inc.* (Ret. Aug. 2023) (Testifying Expert for MediaTek Inc.)
- *Alarm.com v. Vivint, Inc.*, AAA Arbitration No. 01-22-0004-5525 (2023) (Testifying Expert for Vivint, Inc.)
- *Alarm.com v. Vivint, Inc.*, No. 2:23-cv-00004-JRG-RSP (E.D. Tex. 2023) (Testifying Expert for Vivint, Inc.)
- *Sable Networks, Inc. v. CloudFlare, Inc.*, No. 6:21-cv-261 (W.D. Tex. Jan. 2024) (Testifying Expert for CloudFlare, Inc.)
- *Finjan LLC v. Palo Alto Networks, Inc.*, No. 4:14-cv-04908-PJH (N.D. Cal. Ret. Sept. 2022) (Testifying Expert for Finjan LLC.)
- *SNMP Research, Inc. v. Broadcom Inc.*, No. 3:20-CV-451 (E.D. Tenn. Ret. May 2022) (Testifying Expert for SNMP Research)
- Patent Reexamination (U.S.P.T.O. Ret. Mar. 2023) (Testifying Expert for MediaTek)
- *Corrigent Corp. v. Arista Networks, Inc.*, No. 1:22-cv-00497-UNA (D. Del. Ret. Oct. 2022) (Testifying Expert for Arista)
- *GComm v. Samsung*, No. 2:22-cv-0078-JRG (E.D. Tex. Jan. 2024) (Testifying Expert for Samsung)
- *Certain Mobile Telephones, Tablet Computers with Cellular Connectivity, and Smart Watches with Cellular Connectivity, Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1299 (U.S.I.T.C. July 2022) (Testifying Expert for Ericsson)
- *Oasis Tooling, Inc. v. Siemens Indus. Software, Inc.*, No. 1:22-cv-151 (D. Del. Ret. June 2022) (Testifying Expert for Oasis Tooling)
- *Oasis Tooling, Inc. v. GlobalFoundries U.S. Inc.*, No. 1:22-cv-312 (D. Del. Ret. June 2022) (Testifying Expert for Oasis Tooling)
- *NextGen Innovations, LLC v. Infinera Corp.*, No. 2:22-cv-00306-JRG-RSP (E.D. Tex. Ret. Apr. 2023) (Testifying Expert for Infinera)
- *Intellectual Ventures, et al. v. Gen. Motors Co.*, No. 6:21-CV-1088 (W.D. Tex. Jan. 2023) (Testifying Expert for General Motors)
- *Neo Wireless LLC v. Volkswagen Grp. of Am., Inc.* (Sept. 2023) (Testifying Expert for Volkswagen)
- *XR Commc'ns, LLC v. D-Link Sys., Inc.*, No. 8:17-cv-00596 (C.D. Cal.) (Testifying Expert for Hewlett Packard Enterprise)

- *Fundamental Innovation Sys. Int'l LLC v. TCT Mobile (US)*, No. 20-552-RGA-CJB (D. Del. June 2022) (Testifying Expert for TCL)
- Patent Reexamination (U.S.P.T.O. Ret. May 2022) (Testifying Expert for Nokia)
- *Certain Routers, Access Points, Controllers, Network Management Devices, Other Networking Products, and Hardware and Software Components Thereof*, Inv. No. 337-TA-1227 (U.S.I.T.C. Aug. 2021) (Testifying Expert for Hewlett Packard, Netgear, and CommScope)
- *Allied Telesis, Inc. v. Micron Tech., Inc.*, No. 2015-1-CV-282977 (Cal. Super. Ct. Santa Clara Cnty. 2022) (Testifying Expert for Micron)
- *Certain Residential Premises Security Monitoring and Automation Control Panels, and Components Thereof*, Inv. No. 337-TA-1273 (U.S.I.T.C. Apr. 2022) (Testifying Expert for Vivint, Inc.)
- *ADT LLC v. Vivint, Inc.*, No. 6:21-cv-00687 (W.D. Tex. Apr. 2022) (Testifying Expert for Vivint, Inc.)
- Patent Reexamination (U.S.P.T.O. Ret. June 2020) (Testifying Expert for Twitter)
- *Vaxcel Int'l Co., Ltd. v. Heathco LLC*, No. 20-224-LPS (D. Del. Ret. Feb. 2021) (Testifying Expert for Vaxcel)
- *Sable Networks, Inc. v. CloudFlare, Inc.*, No. 6:21-cv-261 (W.D. Tex. Jan. 2024) (Testifying Expert for CloudFlare, Inc.)
- *In re Certain UMTS And LTE Cellular Commc'ns Modules And Prods. Containing The Same*, Inv. No. 337-TA-1240 (U.S.I.T.C. Mar. 2023) (Testifying Expert for Telit Wireless Communication, Quectel, and Thales)
- *ADP, LLC v. Ariz. Dep't of Revenue*, No. TX2018-000246 (June 2020) (Testifying Expert for ADP, LLC)
- *Guzik Tech. Enters. v. Keysight Techs., Inc.*, No. 19CV355879 (Cal. Super. Ct. Santa Clara Cnty. Ret. Aug. 2020) (Testifying Expert for Keysight Technologies, Inc.)
- *Certain High-Density Fiber Optic Equipment and Components Thereof*, Inv. No. 337-TA-1194 (U.S.I.T.C. Oct. 2020) (Testifying Expert for AFL Communications, Panduit, FS.Com, Wirewerk, and Siemon)
- *Huawei Techs. Co. Ltd v. Verizon Commc'ns, Inc.*, No. 2:20-cv-0030 (E.D. Tex. Ret. Mar. 2020) (Testifying Expert for Verizon)
- *Vaxcel Int'l Co., Ltd. v. Jasco Prods. Co., LLC.*, No. 5:19-CV-00154-JD (W.D. Okla. Ret. Aug. 2020) (Testifying Expert for Vaxcel)
- *Bell N. Research LLC v. ZTE*, No. 3:18-cv-01786 (S.D. Cal. Ret. July 2019) (Testifying Expert for ZTE)
- *Bell N. Research LLC v. Kyocera Corp.*, No. 3:18-cv-1785 (S.D. Cal. May 2019) (Testifying Expert for Kyocera)

- *ID Tech Corp. v. Samsung Elecs. Co., Ltd.*, No. 8:17-cv-1748-DOC-JDE (C.D. Cal. Ret. Jan. 2019) (Testifying Expert for Samsung)
- *Parity Networks, LLC v. Juniper Networks, Inc.*, No. 6:17-CV-00495-RWS-KNM (E.D. Tex. Ret. Apr. 2018) (Testifying Expert for Juniper)
- *Parity Networks, LLC v. Hewlett Packard Enter. Co.*, No. 6:17-CV-00682 (E.D. Tex. Ret. Sept. 2018) (Testifying Expert for Hewlett Packard Enterprise Company)
- *NASDAQ v. Miami Int'l* (Ret. Feb. 2018) (Expert for Miami International)
- *Qualcomm v. Apple*, No. 3:17-cv-00108-GPC-MDD (S.D. Cal. Apr. 2019) (Testifying Expert for Qualcomm)
- *Sycamore IP Holdings LLC v. Verizon Commc'ns Inc.*, No. 2:16-cv-591-JRG-RSP (E.D. Tex. Sept. 2017) (Testifying Expert for Verizon and Level 3)
- *Huawei Techs. Co. Ltd. v. Nokia Sols. and Networks*, No. 2:16-cv-0056-JRG-RSP (E.D. Tex. Dec. 2017) (Testifying Expert for Nokia)
- *Huawei Techs. Co. Ltd. v. Samsung Elecs. Co., Ltd.*, No. 3:16-cv-02787 (N.D. Cal. Mar. 2019) (Testifying Expert for Samsung)
- *Nokia v. LG Elecs.*, Int'l Chamber of Commerce Arb. No. 21326 (Oct. 2016) (Testifying Expert for Nokia)
- *Godo Kaisha IP Bridge 1 v. TCL Commc'n Tech. Holdings*, No. 15-634-SLR-SRF (D. Del. Oct. 2018) (Testifying Expert for IP Bridge)
- *Odyssey Wireless, Inc. v. Samsung Elecs. Co., Ltd.*, No. 3:15-cv-1738-H-RBB (S.D. Cal. Oct. 2016) (Testifying Expert for Samsung)
- *Mobile Telecomm. Techs. LLC v. Amazon.com, Inc.*, No. 2:13-cv-883-JRG-RSP (E.D. Tex. Apr. 2015) (Testifying Expert for Amazon)
- *Mobile Telecomm. Techs. LLC v. LG Elecs. Mobilecomm U.S.A., Inc.*, No. 2:13-cv-947-JRG-RSP (E.D. Tex. Feb. 2016) (Testifying Expert for LG Electronics Mobilecomm)
- Inter Parte Reexamination for U.S. Patent Nos. 6,895,520 and 6,899,332 (Feb. 2016) (Expert for LG Electronics)
- *Magna Elecs. Inc. v. TRW Auto. Holdings Corp.*, No. 1:12-cv-00654 (W.D. Mich. Feb. 2016) (Testifying Expert for Magna Electronics)
- *Magna Elecs. Inc. v. TRW Auto. Holdings Corp.*, No. 1:13-cv-00324 (W.D. Mich. Feb. 2016) (Testifying Expert for Magna Electronics)
- *Wi-LAN USA, Inc. v. Telefonaktiebolaget LM Ericsson*, No. 1:12-cv-23569 (S.D. Fla. May 2015) (Testifying Expert for Wi-LAN)
- *Wi-LAN USA, Inc. v. Alcatel-Lucent USA, Inc.*, No. 1:12-cv-23568-Altonaga/Simonton (S.D. Fla. May 2015) (Testifying Expert for Wi-LAN)

13. My opinions as set forth herein are based on my experience as well as my investigation and study of materials relevant to this case. In formulating my opinions, I have reviewed the materials I discuss herein, as well as the following: the '305 Patent and the '788 Patent; the file history to the '305 Patent and the '788 Patent; the parties' P.R. 4-1 Proposed Terms for Construction; Plaintiff's Disclosure of Preliminary Claim Constructions and Extrinsic Evidence Under P.R. 4-2, including Exhibit A thereto and the extrinsic evidence cited therein; and Innolux's P.R. 4-2 Preliminary Claim Constructions and Preliminary Identification of Extrinsic Evidence, and the extrinsic evidence cited therein.

II. Legal Standards

14. I am not a lawyer, and I do not intend to offer any opinions on the correct interpretation of the law. Counsel for Innolux has informed me of the relevant standards for claim construction, and I have applied them to the best of my ability.

15. I understand that patent claim construction is a question of law for the Court. The claims in a patent define the patent's scope and thus the rights of the patentee to exclude others from making, using, or selling the invention. I also understand that in order to determine patent infringement, the claims must first be construed to determine their proper meaning.

16. I am informed that claim construction begins with the presumption that claim terms are given their ordinary and customary meaning, which is the meaning they would have to a POSA at the time of the invention. I have been informed that an analysis of the level of ordinary skill in the art may be based, in part, upon the educational level of those working in the field, the sophistication of the technology, the problems encountered, the state of the art, the prior art solutions to those problems, and the speed at which innovations were being made at the time of the filing of the application which led to the patent. I am informed that to determine the ordinary

and customary meaning of a term, the Court may consult several sources of information. This information includes the “intrinsic record,” i.e., the claims themselves, the specification, and the prosecution history of the patent. The Court may also consult “extrinsic evidence” such as relevant dictionaries, treatises, and expert testimony, which can be relied on to the extent that it is not inconsistent with the intrinsic record.

17. I am informed that a claim term must be understood in the context of the patent as a whole, including the remaining terms, the specification, and the prosecution history. I am informed that it is not proper to read limitations from described embodiments in the specification into the claim terms, or to read express limitations out of the claims. However, I am informed that the usage of a claim term in the remaining claims, the specification, and the prosecution history may provide guidance as to the intended meaning of a claim term. I also understand that terms may be defined in the patent in a way that is different from the meaning they would otherwise possess; in those circumstances, the definition provided in the patent governs. I understand that the specification of a patent is always highly relevant to the claim construction analysis. I am informed that, usually, the specification is dispositive, meaning that it is the single best guide to the meaning of a disputed term. I am also informed that the construction that stays true to the claim language and most naturally aligns with the patent’s description of the invention will be the correct construction. I am further informed that unless the inventor intended a term to cover more than the ordinary and customary meaning revealed by the context of the intrinsic record, it is improper to read the term to encompass a broader definition simply because it may be found in a dictionary, treatise, or other extrinsic source.

18. I am informed that claims should be interpreted so as to preserve their validity. However, I am also informed that claims should only be interpreted to preserve their validity if, after applying all the other tools of claim construction, a patent term is still ambiguous.

19. I am informed that claim terms must be sufficiently definite, so that a POSA would understand the bounds of the claim when read in light of the specification. I am further informed that absolute precision is unattainable in claims, but that the claims must provide reasonable certainty as to their scope to the POSA.

20. I am informed that a patent may describe a claim limitation as a means for performing a function, rather than as a particular structure. I am informed that this is referred to as “means-plus-function” claiming. I am informed that there is a presumption that a claim which uses the term “means” is a means-plus-function claim. I am also informed that there is a presumption that a claim which does not use the term “means” is not a means-plus-function claim.

21. I am informed that if a claim uses a means-plus-function term then proper interpretation of the term is a two-step process. First, the function of the claim is identified. Second, structure corresponding to that function is identified in the patent specification. The claim is understood to be limited to the structures described in the specification corresponding to the function. I am informed that if the patent specification does not describe structure that a person of ordinary skill would understand to be sufficient to perform the claimed function, then the claim is indefinite.

22. I am informed that when a patent claim uses means-plus-function claiming, the associated function may be a computer-implemented function. In that case, I am informed that a description of general-purpose computer equipment is insufficient to provide corresponding

structure to that function. I am informed that the proper structure to identify is an algorithm for performing the computer-implemented function. I understand that an algorithm may be described in prose, in a flow chart, in code, in pseudocode, or in any other method that a POSA would understand. I am informed that a “black box” recitation of structure is insufficient to support a means-plus-function claim. I am further informed that some description of the internal circuitry of a “black box,” or of the algorithm performed by a “black box,” is required.

III. Level of Ordinary Skill in the Art

23. In my opinion, a person of ordinary skill in the art (POSA) of the Asserted Patents as of the purported priority date (June 11, 2003) would have had at least a bachelor of science degree in physics, electrical engineering, or the equivalent thereof and three (3) years of experience in circuit design or display technologies. Such a POSA would have had knowledge of integrated circuits, gamma correction, and storage of gamma correction voltage values within memory, and would have understood how to search available literature for relevant publications.

24. I understand that the application that issued as the ‘305 Patent was filed in December 2003 and claims priority to a provisional application filed in June 2003. At either time, I satisfy the definition of a POSA. I now consider myself an expert in the relevant field of technology for the ‘305 patent.

25. I understand that the application that issued as the ‘788 Patent was filed in May 2007 and claims priority to a provisional application filed in June 2003. At either time, I satisfy the definition of a POSA. I now consider myself an expert in the relevant field of technology for the ‘788 patent.

26. In forming my opinions for this Declaration, I have used the perspective of one of ordinary skill in the art as defined above. My opinions contained herein, however, would not be affected if a POSA is defined as someone who has slightly more or slightly less experience than defined above.

IV. Technology and Claim Terms of the Asserted Patent

27. Innolux has asked me to provide expert testimony regarding the understanding of a POSA of the Asserted Patents at the time of the purported invention of the meaning of certain claim terms and limitations within the Asserted Claims in light of the intrinsic evidence (claims, specification, and prosecution history) and extrinsic evidence.

28. In the following paragraphs I provide my interpretations as I believe one of ordinary skill in the art would understand these disputed claim terms at the time of the purported invention (June 2003). I have reviewed and agree with Innolux's claim construction positions regarding the Asserted Claims in the Patent Local Rule 4-3 Disclosure dated May 8, 2025, and incorporate that Disclosure in this Declaration by reference. I have also considered and taken into account Phenix's claim construction positions. I reserve the right to supplement this Declaration to address any further explanation by Phenix and/or its expert of its claim construction contentions and/or arguments in briefing, and to supplement this Declaration to the extent Phenix changes any of the constructions proposed in the Disclosure.

A. '305 Patent

1. Non-volatile storage cells

Innolux Proposed Construction	AUO Proposed Construction	Phenix Proposed Construction
analog memory cells which retain stored data even when power is removed	(same as Innolux)	memory cells which retain stored data even when power is removed

29. It is my opinion that the term “non-volatile storage cells,” as used in U.S. Patent No. 7,123,305 (the “‘305 patent”), refers to Analog memory cells. The patent’s disclosures consistently point to an analog interpretation, and the functional requirements described and claimed appear to necessitate such an interpretation. An alternative construction, particularly one that includes digital memory cells, would conflict with multiple explicit teachings within the ‘305 patent.

30. The specification of the ‘305 patent uses direct and unambiguous terminology that identifies the nature of its storage cells as analog. The specification explicitly identifies the memory elements as “programmable analog floating gate memory cells 330 through 337” (3:51-52) and “an analog storage cell” (4:4). Such direct terminology expressly identifies that the “non-volatile storage cells” of the claims are analog memory cells.

31. Furthermore, the specification states: “Each output is internally connected to an analog storage cell which can be written with analog values, for example, of 1024 step (10 Bit) resolution.” (4:4-6). An embodiment is later described where “[e]ach output is internally connected to an analog nonvolatile storage cell which can be written with 1,024 analog values, providing 10 bit resolution, or, said another way, to better than 15 mV resolution.” (5:40-43). These descriptions directly associate the storage cells with the storage of “analog values” at specified precision levels. The specification also explains that during programming, “the value of the Analog Input is written

into the nonvolatile memory for the output channel selected by the A2-A0 inputs.” (3:25-29). The direct writing of an “Analog Input” value into the memory cells further suggests that these are Analog memory cells designed to store such analog quantities.

32. The patent does not describe any embodiment where the “non-volatile storage cells” store digital data that is subsequently converted to an analog signal. The consistent focus on direct analog storage capabilities across all disclosed embodiments leads a POSA to understand the term “non-volatile storage cells” in the ‘305 Patent as referring to solely to analog memory cells.

33. The language of the patent claims further supports the view that the “non-volatile storage cells” are analog memory cells. Claim 1 of the ‘305 Patent recites “drivers connected to said storage cells and to the plurality of outputs.” A POSA would understand “drivers” in integrated circuits as elements that take an input signal and provide it with appropriate power to drive subsequent circuitry. Indeed, I understand the parties have agreed that the term “drivers” refers to buffers or amplifiers. In Claim 1, these drivers connect to the “plurality of outputs” to provide “voltage signals,” which are the analog gamma reference voltages. The phrase “drivers connected to said storage cells” implies a direct functional connection, as I separately discuss below. Further, the Figures of the ‘305 patent do not depict any intervening components between the memory cells and the drivers. *See, e.g.* Figs. 3, 6. For the drivers to output analog “voltage signals,” the signal they receive from the “storage cells” must itself be an analog voltage. Thus, “non-volatile storage cells” would be understood as analog memory cells, which store and output such analog voltage signals directly to connected drivers.

34. Moreover, if “non-volatile storage cells” were interpreted as digital memory cells storing numeric data (e.g., binary codes), a POSA would recognize that drivers could not directly

process such digital data to produce the required analog gamma reference voltages. An intermediate Digital-to-Analog Converter (DAC) would be essential to convert stored digital data into an analog voltage before the output drivers could process that voltage. No such embodiment is shown or even suggested in the specification. In such a scenario, the drivers would connect to the DAC's output, not directly to the digital memory cells. This configuration would contradict the explicit language of Claim 1, which requires "drivers connected to said storage cells."

35. Claim 4 of the '305 Patent, dependent on Claim 1, further confirms this understanding. Claim 4 recites: "The integrated circuit of claim 1 wherein said non-volatile storage cells hold analog voltage values which are a constant fraction of said gamma reference voltage signals." (8:1-4). This explicit statement that the cells "hold analog voltage values" dictates the interpretation derived from Claim 1. The "data" retained by these cells is expressly identified as "analog voltage values."

36. Claim 6 of the '305 Patent, a method claim for programming the integrated circuit of Claim 1, also confirms a POSA's understanding that the claimed non-voltage storage cells must be Analog memory cells. Claim 6 includes the step of "programming an applied gamma voltage in the selected storage cell by applying incremental voltage pulses from the programming pin." (8:18-21). A POSA would recognize that programming a memory cell to store an "applied gamma voltage" (an analog quantity) using "incremental voltage pulses" is a technique characteristic of precisely setting and storing analog voltage levels in analog memory cells. This method allows for fine adjustments to reach a specific target analog voltage, which differs from typical methods for storing discrete digital (binary) values.

37. The drawings included in the '305 Patent also dictate interpreting the "non-volatile storage cells" as analog memory cells. Figures 3 and 6 depict memory elements (e.g., elements

330-337 in Figure 3) directly connected to driver elements (e.g., element 340 in Figure 3) without any intervening components. This direct connection, as illustrated, is consistent with the cells being analog memory cells that output analog voltage signals directly to the drivers. The specification explicitly identifies these depicted elements as “programmable analog floating gate memory cells 330 through 337.” (3:51-52). A POSA would recognize these symbols, along with their explicit description, as representing a specific type of analog storage device, distinct from generic symbols typically associated with standard digital memory cells (such as SRAM, DRAM, or digital ROM/EEPROM).

38. Notably, a review of the ‘305 Patent, including its figures, reveals no teaching, suggestion, or depiction of a Digital-to-Analog Converter (DAC) positioned between the “non-volatile storage cells” and the “drivers.” As discussed in relation to Claim 1, if the “non-volatile storage cells” were digital, a DAC would be an essential component. Its absence in the patent figures strongly supports the understanding that the cells are inherently analog, designed to provide analog voltage values directly to the drivers. Furthermore, Figure 4B illustrates the programming circuitry for the analog memory cells, detailing the mechanisms for applying the programming pulses described in the specification. This programming architecture is consistent with analog storage techniques rather than common digital memory programming approaches, further supporting the interpretation that the “non-volatile storage cells” are analog memory cells.

39. The context of the ‘305 Patent, including the problem it aims to solve and its differentiation from prior art, indicates an intentional analog approach, which further solidifies the understanding that its “non-volatile storage cells” are analog memory cells. The specification characterizes the generation of gamma correction voltages as an “‘analog’ problem.” (2:8). A POSA would typically understand this to mean that the core technical challenge lies in accurately

producing and controlling continuous analog voltage levels. The invention described in the ‘305 Patent is presented as a direct solution to this “analog problem” by storing and outputting precise analog voltage values.

40. The ‘305 Patent’s discussion of certain prior art reinforces this view. It identifies U.S. Patent No. 6,593,934 to Liaw et al. (“Liaw”) and U.S. Patent No. 6,046,719 to Dingwall (“Dingwall”) as examples of prior art that “teach quite complex digital approaches to this ‘analog’ problem; consequently both inventions are quite expensive.” (‘305 Patent, 2:4-9). The ‘305 Patent’s explicit criticism of these digital approaches as “complex” and “expensive,” and its stated objective to provide a solution that “achieves acceptable cost” (‘305 Patent, 2:10-12), would lead a POSA to conclude that the ‘305 Patent’s invention employs analog memory cells as a distinct and advantageous alternative to such digital storage approaches.

41. This interpretation is further supported by the Applicant’s arguments during the prosecution of the related U.S. Patent No. 7,557,788 (the “‘788 Patent”), a continuation of the application that led to the ‘305 Patent. In distinguishing the invention claimed in the ‘788 Patent from Liaw, the Applicant characterized Liaw as disclosing an “automatic Gamma parameter correction system with a digital/analog converter (DAC)” (Applicant’s Remarks dated October 22, 2008, in ‘788 Patent prosecution, p. 9). In contrast, the Applicant described their invention in terms of directly “storing said applied gamma voltages in reprogrammable, nonvolatile cells” (Id., p. 8). A POSA would likely view this distinction—emphasizing direct analog storage versus a DAC-based digital system—as consistent with the ‘305 Patent’s own critique of “complex digital approaches” and as additional evidence that its “non-volatile storage cells” are analog memory cells.

42. The programming methodology described in the ‘305 Patent specification is also characteristic of programming analog memory cells. The specification details the use of a high voltage input, VPP, which “provides the programming voltage and timings needed to program the analog memory cells” and “provides the high voltage pulses used to program the individual cells.” (4:29-32, 6:27-30). One method described involves “programming of the selected storage cell ... by pulsing VPP with adjustable voltage pulses between approximately 8 and 14 volts.” (6:45-48). A POSA would understand that applying an analog input voltage (as previously discussed) and using adjustable high voltage pulses to store that precise analog level are techniques for programming Analog memory cells, distinct from typical digital memory programming focused on writing discrete logic levels.

43. Extrinsic evidence, including general technical principles and relevant literature from the time, further aligns with and supports the interpretation of the “non-volatile storage cells” in the ‘305 Patent as analog memory cells. A POSA would possess foundational knowledge that analog memory cells are specifically designed to store a continuous or multi-level range of analog values (e.g., a specific voltage level) directly as their retained data. This contrasts with digital NVM cells, which are designed to store discrete values (typically a logical ‘0’ or ‘1’). This fundamental distinction supports the view that the “non-volatile storage cells” of the ‘305 Patent, which are consistently described as storing and outputting analog voltages without an intervening DAC, are indeed analog memory cells.

44. General technical literature available to a POSA at the time also corroborates this understanding. For instance, a comprehensive guide such as *Nonvolatile Semiconductor Memory Technology: A Comprehensive Guide to Understanding and Using NVSM Devices*, edited by William D. Brown et al. (Wiley-IEEE Press 1997) (“Brown”), provides information on various

NVSM devices. Such literature typically depicts standard symbols for different types of memory cells, many of which are digital. A POSA would likely observe that the specific, non-conventional symbols used in the ‘305 Patent’s drawings (e.g., Fig. 3, elements 330-337), which the patent explicitly describes as “programmable analog floating gate memory cells” (3:51-52), are not found among the standard memory cell symbols illustrated in a general reference like Brown (e.g., Brown at Figs. 1.21, 1.24, 1.26, 1.28, 1.32, 1.37, 1.42).

45. This discrepancy would suggest to a POSA that the ‘305 Patent is not referring to generic digital cells commonly represented by standard symbols, but rather to a specialized type of analog memory cell. Therefore, when considering general technical literature alongside the ‘305 Patent’s specific disclosures, its explicit terminology, and its unique drawings, the understanding that the “non-volatile storage cells” of the ‘305 Patent are analog memory cells is reinforced, rather than implying a broad encompassment of any NVSM device including standard digital cells.

2. *Connected to / Coupled to*

Innolux Proposed Construction	AUO Proposed Construction	Phenix Proposed Construction
“coupled to” means “indirectly or directly linked or joined” “connected to” means “directly and/or physically linked or joined”	(same as Innolux)	“coupled to”: No construction necessary; plain and ordinary meaning. “connected to”: No construction necessary; plain and ordinary meaning.

46. A person of ordinary skill in the art (POSA) at the time of the invention would understand this distinction. Claim 1 recites, among other limitations, “circuits for programming coupled to a multiplexer,” “drivers connected to said storage cells and to the plurality of outputs,” and “the plurality of inputs connected to said multiplexer.”

47. A POSA would understand that in Claim 1, the phrase “drivers connected to said storage cells and to the plurality of outputs” indicates a direct physical or electrical connection. In integrated circuits such as those generating gamma reference voltages, drivers are circuit elements that take an input signal and provide it with appropriate power, current, or buffering to drive subsequent circuitry. The phrase “drivers connected to said storage cells” indicates a direct electrical path between these components, allowing signals to flow directly from the storage cells to the drivers and then to the outputs. Similarly, a POSA would recognize that “the plurality of inputs connected to said multiplexer” describes a direct connection between input pins and the multiplexer circuit.

48. In contrast, a POSA would understand that the claim’s use of “coupled to” in the phrase “circuits for programming coupled to a multiplexer” suggests a broader functional relationship. This distinction is significant in integrated circuit design, where components may interact through various intermediate elements or shared connections. The phrase indicates that these components work together functionally without necessarily specifying a direct wire-to-wire connection.

49. I have been instructed by attorneys for Innolux that under the principle of claim differentiation, when different terms are used in the same claim, they are ordinarily understood to have different meanings. This legal principle aligns with the technical understanding that a POSA would derive from reading the claim language, where “connected to” describes direct physical links while “coupled to” encompasses broader functional relationships.

50. The ‘305 patent specification consistently maintains this distinction between “connected to” and “coupled to.”. When describing physical relationships between components, the specification consistently uses “connected to” for direct physical connections and “coupled to”

for functional relationships that may involve intermediate components. This pattern is evident throughout the document.

51. The specification says “[t]he programming engine 310, coupled to the mux, comprises an Analog Input which will be used to set the reference voltage level and a R/W control signal for a corresponding gamma reference controller” (‘305 Patent, 3:51–54). Figure 3 illustrates this relationship, showing that the programming engine 310 interfaces with the mux 320 through multiple signal paths and potentially intermediate components, not through a simple direct connection. The choice of “coupled to” here indicates a functional relationship rather than a direct physical connection.

52. In contrast, the specification uses “connected to” when describing direct physical links: “[e]ach output is internally connected to an analog storage cell . . .” (‘305 Patent, 4:4–6). Figure 3 confirms this direct relationship, showing outputs CHO-CH7 directly connected to their respective memory cells through drivers without intermediate components. The specification repeats this direct connection language: “[e]ach output is internally connected to an analog nonvolatile storage cell . . .” (‘305 Patent, 5:40–43) reinforcing that “connected to” means a direct link.

53. The specification also says “[i]n FIG. 3, the channel 0, CH0, is driven by a driver 340, which connects to the programmable analog floating gate memory cells 330. The channel 1, CH1, is driven by a driver 341, which connects to the programmable analog floating gate memory cells 331” (‘305 Patent, 3:61–67). Here again, Figure 3 shows a direct line between driver 340 and memory cell 330, with no intervening components. This consistent pattern of usage reinforces the understanding that “connected to” refers to direct physical connections, while “coupled to”

refers to functional relationships that may involve intermediate components or more complex signal paths.

54. The figures of the '305 patent provide visual confirmation of the distinction between "connected to" and "coupled to." Figure 3, which illustrates one embodiment of a gamma reference controller, clearly shows different types of connections between components. The programming engine (element 310) and the mux (element 320) are shown with multiple signal lines between them, illustrating a functional relationship rather than a simple direct connection. This visual representation matches the specification's description of these components being "coupled to" each other.

55. In contrast, the drivers (elements 340-347) and their respective memory cells (elements 330-337) are shown with direct, single-line connections. Similarly, the connections between the outputs (CH0, CH1, etc.) and their respective drivers are represented as direct lines. These direct connections align with the specification's consistent use of "connected to" or "connects to" when describing these relationships. The mux (element 320) is depicted as having multiple connection paths to the various memory cells, allowing it to route signals to any selected cell. This more complex relationship is consistent with the broader meaning of "coupled to," where components have a functional relationship that may not be a simple direct connection.

56. A POSA's understanding of the terms "connected to" and "coupled to" in the '305 Patent would be informed by general technical principles and authoritative references in the field of electrical engineering. These external sources would confirm the distinct meanings that a POSA would derive from the patent's intrinsic evidence.

57. This technical understanding would be further validated if a POSA consulted general-purpose dictionaries like The American Heritage College Dictionary (3rd Edition, 1997). There, terms related to “connect” are defined in ways that emphasize direct joining: “conjoin” is defined as “to join or become joined together; unite,” and “conjunction” is defined as “the act of joining; combination” and “the state of being joined.” This aligns with the direct physical connection interpretation of “connected to” in the ‘305 Patent.

58. A POSA would note that, in contrast, the same dictionary defines terms related to “couple” with broader meanings that encompass functional relationships. “Couple” is defined as “a device that links or joins two things together.” Significantly, “coupling” is defined specifically in electronics as “the transfer of energy from one circuit to another.” This specialized electronics definition would strongly confirm a POSA’s understanding that in the context of circuit design, “coupling” refers to energy transfer relationships rather than just physical connections.

59. In my experience in the field of integrated circuit design, these distinctions reflect common industry practice. When engineers specify that components are “connected to” each other, they are indicating a direct electrical connection with a continuous conductive path between the elements. When engineers specify that components are “coupled to” each other, they are indicating a functional relationship that may involve intermediate components or more complex signal paths.

3. *Multiplexer*

Innolux Proposed Construction	AUO Proposed Construction	Phenix Proposed Construction
one or more circuits that couple (1) one input (or one set of inputs) to one of many outputs (or one set of many sets of outputs) or (2) one of many inputs (or one set of	One or more circuits, excluding an I2C serial bus, that couple (1) one input (or one set of inputs) to one of many outputs (or one set of many sets of outputs) or (2)	one or more circuits that selectively couple (1) one input (or one set of inputs) to one of many outputs (or one set of many sets of outputs) or (2) one of many inputs (or

many sets of inputs) to one output (or one set of outputs)	one of many inputs (or one set of many sets of inputs) to one output (or one set of outputs)	one set of many sets of inputs) to one output (or one set of outputs)
--	--	---

60. Innolux proposes that the term “multiplexer” as used in Claim 1 of the ‘305 patent (“circuits for programming coupled to a multiplexer for addressing and programming said storage cells”) and Claim 8 (“an output pin connected to an output through a second multiplexer connected to said plurality of outputs”) should be construed as:

“one or more circuits that couple (1) one input (or one set of inputs) to one of many outputs (or one set of many sets of outputs) or (2) one of many inputs (or one set of many sets of inputs) to one output (or one set of outputs).”

61. The ‘305 patent itself applies the term “multiplexer” to distinct circuit elements performing different, and in fact opposite, types of signal routing functions. Claim 1 recites “a multiplexer for addressing and programming said storage cells.” The ‘305 patent specification clarifies this function. For instance, Figure 3 depicts “a mux 320” which “connects signals from the programming engine 310 to any one of the programmable analog floating gate memory cells 330 through 337.” (‘305 patent, 3:55-58). This describes a one-to-many signal routing function, characteristic of what is formally known as a demultiplexer. Figure 6 similarly shows a “Programming Multiplexer” that takes various control and data signals (e.g., from VPP, Analog In, address lines A0-A1, B0-B2) and routes them to selected “Analog Memory Cells” within the “Memory Array.” (‘305 patent, Fig. 6; 6:22-53). This, too, is a one-to-many operation.

62. In contrast, Claim 8 recites “an output pin connected to an output through a **second multiplexer** connected to said plurality of outputs.” This “second multiplexer” performs a many-to-one function. Figure 6 shows this distinct output multiplexer selecting one channel from “CH0

. . . CH17” (many inputs) to be output to the “AOUT” (Analog Output) pin (one output). (‘305 patent, Fig. 6). The patent’s pin descriptions state, “AOUT Outputs the current value of the selected channel of the selected bank during programming.” (‘305 patent, Fig. 4A Pin Descriptions). This is a classic many-to-one multiplexer function.

63. Thus, the ‘305 Patent’s own lexicography uses the single term “multiplexer” (or “mux”) as a label for components with fixed one-to-many functionality and for other components with fixed many-to-one functionality. The patent does not limit the term to only one of these operations.

64. A Person of Ordinary Skill in the Art (POSA) at the time of the invention would interpret the term “multiplexer” by first looking at its usage within the patent itself, and then considering the broader context of the art. A POSA would be aware of the formal, distinct definitions for these types of devices. For example, IEEE Std 100-2000, *The IEEE Standard Dictionary of Electrical and Electronics Terms*, 7th ed. (New York: IEEE, 2000) (“IEEE Dictionary”), defines “multiplexer” primarily as a device performing a many-to-one operation: “(A) (supervisory control) A device that interleaves signals to a single line, or selects one input and switches its information to the output.” (IEEE Dictionary at 716). The same dictionary defines “demultiplexer” as a device performing a one-to-many operation: “(A) (data transmission) A device used to separate two or more signals that were previously combined by a compatible multiplexer and transmitted over a single channel.” (IEEE Dictionary at 288).

65. Despite these formal distinctions, a POSA would also know from practical experience and common engineering parlance that the term “multiplexer” is sometimes used in a more casual, generic sense to refer to either a device that performs a many-to-one selection (a formal multiplexer) or a device that performs a one-to-many distribution (a formal demultiplexer).

66. Seeing that the ‘305 Patent itself applies the term “multiplexer” to components performing both these distinct functions (as established above), a POSA would understand that the patentee is using “multiplexer” in this common, broader, generic sense. The patent’s usage as its own lexicographer is consistent with how POSAs often practically apply the term. Therefore, Innolux’s proposed construction, which defines “multiplexer” as a circuit that can perform *either* a one-to-many function *or* a many-to-one function, accurately captures this patent-specific lexicography, which mirrors a known general usage in the art.

67. I understand that Phenix proposes a construction that inserts the word “selectively,” proposing: “one or more circuits that *selectively* couple (1) one input (or one set of inputs) to one of many outputs . . .” (emphasis added). While a POSA (and this patent) might use “multiplexer” generically to refer to *either* a many-to-one or a one-to-many fixed-function device, this generic usage does not imply that a single device simply labeled a “multiplexer” is inherently a special, more complex component that can *selectively switch* its fundamental mode of operation (e.g., from being a many-to-one device to being a one-to-many device, or vice-versa). In my opinion, if the inventors of the ‘305 Patent intended such a switchable or bidirectional functionality, it would require explicit description or clear contextual support in the patent.

68. The ‘305 Patent provides no disclosure whatsoever of any such switchable multiplexer. As shown, the “multiplexer for addressing and programming” (e.g., mux 320, Programming Multiplexer in Fig. 3 and Fig. 6) performs a one-to-many function, and the physically distinct “second multiplexer” for output (Fig. 6) performs a many-to-one function. These are described as separate components with distinct, fixed roles. There is no teaching or suggestion that either of these components, or any other component called a “multiplexer” in the patent, can change its mode of operation.

69. In my view, Phenix’s proposed insertion of “selectively” is an attempt to improperly import this un-disclosed switchable characteristic into the general term “multiplexer.” This would wrongly limit the term to a specific type of advanced, mode-selectable multiplexer not described or claimed in the ‘305 Patent. A POSA, seeing the term “multiplexer” used in the patent to describe different fixed-function components, would not conclude that the patent refers to a single, selectively mode-switching device. Adding “selectively” imposes a functional limitation (the ability to choose its mode of operation) that lack any basis in the patent’s disclosure.

4. *External source for the high voltage programming means*

Innolux Proposed Construction	AUO Proposed Construction	Phenix Proposed Construction
a voltage source for the high voltage programming means that is not inside or a part of the claimed integrated circuit	(No specific construction offered by AUO)	No construction necessary; plain and ordinary meaning

70. Claim 5 of the ‘305 Patent recites “The integrated circuit of claim 1 wherein said circuits for programming require an external source for the high voltage programming means.” A person of ordinary skill in the art (POSA) at the time of the invention would understand “external source” as used in this claim to refer to a source that is not inside or a part of the claimed integrated circuit. To be clear, it is my opinion that this represents the plain and ordinary meaning as a POSA would understand that claim language in light of the specification.

71. This understanding is directly supported by the plain language of the claim. The claim expressly differentiates between the “integrated circuit” and the “external source,” indicating that the source is external to—that is, outside of—the integrated circuit itself. The phrase “external source for the high voltage programming means” thus indicates that the high voltage needed for

programming the storage cells must originate from outside the claimed integrated circuit, not from within it.

72. A POSA would interpret this claim limitation as establishing that the high voltage signals necessary for programming the non-volatile storage cells must be provided from outside the integrated circuit rather than being generated internally. This understanding follows from the ordinary technical meaning of “external” as something that exists or originates outside of a defined boundary—in this case, outside the boundaries of the integrated circuit described in claim 1.

73. The specification of the ‘305 Patent consistently describes the high voltage programming source (Vpp) as being external to the integrated circuit, which supports the interpretation that “external source” refers to a source that is not inside or a part of the claimed integrated circuit.

74. In describing an embodiment of the invention (the AG 1818), the specification explicitly states: “The Vpp is a high voltage input used to select the programming mode and also provides the high voltage pulses used to program the individual cells. In the AG 1818 embodiment, Vpp is supplied from an external source, an IC or other means.” (6:25-29). This statement directly supports the understanding that “external source” means a source that is not inside or a part of the claimed integrated circuit, as it explicitly describes Vpp as being “supplied from an external source.”

75. The specification further reinforces this interpretation by detailing the programming process where Vpp is an input to the integrated circuit: “The programming interface consists of four signals. The Vpp is a high voltage input used to select the programming mode and also provides the high voltage pulses used to program the individual cells.” (6:22-26). By

describing Vpp as an “input,” the specification indicates that this signal enters the integrated circuit from outside, rather than being generated internally.

76. Figure 4A in the patent also lists Vpp as one of the pin descriptions, identifying it as “Programming Voltage” with a value range of “10-14Volts.” (4:28). Figure 4B further shows Vpp as an input pin to the device. This representation of Vpp as an input pin on the integrated circuit reinforces that the high voltage is supplied from an external source, not generated within the integrated circuit.

77. The specification describes a programming method that involves “pulsing Vpp with adjustable voltage pulses between approximately 8 and 14 volts.” (6:45-47). These relatively high voltages (compared to the typical 3-5V operating voltages mentioned elsewhere in the specification) are characteristic of the programming voltages required for non-volatile memory cells. A POSA would understand that generating such high voltages on-chip would require specialized high-voltage circuitry that, if present, would have been described in the specification. The absence of any description of on-chip high-voltage generation circuitry, coupled with the explicit statement that Vpp is “supplied from an external source,” confirms that the high voltage programming means requires an external source.

78. The specification also mentions alternative sources for the Vpp signals: “A PC based programming interface is available for prototyping and gamma optimization. This PC programming interface may be an alternative source of the Vpp signals.” (7:12-14). This further supports the understanding that the Vpp signal comes from an external source, as it describes a PC-based interface as a possible source for these signals.

79. The figures of the '305 Patent provide additional support for the interpretation that "external source" refers to a source that is not inside or a part of the claimed integrated circuit.

80. Figure 4A shows a table of pin descriptions for the integrated circuit, which includes "Vpp" described as "Programming Voltage" with a value range of "10-14Volts." The description states that Vpp "[p]rovides the programming voltage and timings needed to program the analog memory cells. Also used to enter programming modes other than read." (4:28-32). By describing Vpp as a pin with specific input voltage characteristics, Figure 4A reinforces that this high voltage comes from an external source.

81. Figure 4B illustrates the physical pinout of the integrated circuit, showing "VPP" as one of the input pins. This visual representation clearly indicates that Vpp is an input to the integrated circuit from an external source, not a voltage generated internally.

82. Figure 3, which shows a block diagram of the gamma reference controller, does not show any internal high-voltage generation circuitry, further supporting the understanding that the high voltage for programming is provided externally.

83. A POSA's understanding of the term "external source for the high voltage programming means" in the '305 Patent is informed by general technical principles related to programming non-volatile memory devices, particularly in the context of integrated circuits designed for display applications.

84. Non-volatile memory technologies, including those used in the '305 Patent's analog memory cells, typically require higher voltages for programming (writing) operations than for normal read operations. These programming voltages are often in the range of 8-14V, as mentioned in the '305 Patent (6:45-47), while normal operating voltages for integrated circuits are

typically 3-5V. Generating these higher voltages on-chip requires specialized circuitry (such as charge pumps) that consume significant die area and power.

85. For cost-sensitive applications like display drivers, it is common practice to provide programming voltages from an external source rather than generating them on-chip. This approach reduces the cost, complexity, and size of the integrated circuit. The '305 Patent follows this established practice by specifying that the high voltage for programming is supplied from an external source.

86. Extrinsic evidence, such as the data sheets for similar programmable devices from the relevant time period (e.g., Intel's 2816A EEPROM and Microchip's PS40X series), shows that it was common practice to provide programming voltages from external sources. For example, these devices typically had dedicated Vpp pins for accepting programming voltages from external power supplies or programming equipment.

87. The patent's express statement that the "Vpp is supplied from an external source, an IC or other means" (6:27-29) uses terminology that a POSA would understand as referring to sources outside the integrated circuit itself. This is consistent with how similar terms were used in the field at the time, where "external" clearly meant outside the boundaries of the integrated circuit in question.

88. Contemporaneous technical literature confirms this ordinary understanding. The 1983 Intel 2816A data sheet, for example, designates a dedicated VPP pin that must be driven with approximately 12.5 volts from an off-chip programmer during erase or write operations, whereas the device operates at only 5 volts in normal mode. A POSA would recognize that the very

presence of these separate high-voltage pin signals that the programming energy is expected to be supplied by equipment external to the integrated circuit.

89. The same practice is expressly described in Microchip Technologies' PS40X-02XX Programming Guide (2002). When explaining how to update the on-chip one-time-programmable (OTP) block, the manual states that the user block "can be updated ... **using an external programming voltage for access,**" and the accompanying block diagram shows a VPP pin feeding the device. Again, the high-voltage supply is assumed to reside outside the IC.

90. Contemporary patents reinforce this view. Edme et al., U.S. Patent No. 5,175,706, notes that "the programming voltage VPP is given by an external supply" (1:14-26) before contrasting that arrangement with designs that integrate charge pumps on-chip. Lisart et al., U.S. Patent No. 5,889,720, likewise explains that an "external supply circuit ... produces this high voltage" (3:18-35) of roughly 20 V needed to program floating-gate memories. Fazio, U.S. Patent No. 5,677,869, describes flash memory cells that are programmed with gate voltages of about 12 V supplied through the device's VPP pin by external test equipment (see, e.g., Figs. 4-5 and accompanying text). Each of these references depicts the same architectural choice: the high-voltage programming potential is generated off-chip and delivered to the integrated circuit via a dedicated pin.

91. Taken together, these data sheets and patents demonstrate that, at the time of the alleged '305 invention, designers of non-volatile memories routinely relied on a voltage source physically outside the chip to furnish the VPP level necessary for programming. A POSA would therefore read the claim phrase "external source for the high voltage programming means" as entirely consistent with—and indeed reflecting—the prevailing industry practice of sourcing the programming voltage off-chip, which would in this case represent the plain and ordinary meaning.

Furthermore, if “external source” were not interpreted to mean “external to the integrated circuit,” the claim language would become indefinite, as there would be no clear reference point for what the source is “external” to. The term “external” inherently establishes a boundary relationship—something is outside of something else. In the context of an integrated circuit claim, the natural and only reasonable boundary is the integrated circuit itself. Any alternative interpretation would leave a POSA unable to determine the scope of the claim, as there would be no discernible boundary to define what constitutes “external.” The specification consistently treats the programming voltage as being supplied from outside the integrated circuit through an input pin, and never suggests any alternative boundary or reference point for the term “external.” Therefore, interpreting “external source” as meaning “a source that is not inside or a part of the claimed integrated circuit” is not only supported by the intrinsic and extrinsic evidence, but is also the only interpretation that avoids rendering the claim indefinite.

B. ‘788 Patent

1. *Gamma reference control capability*

Innolux Proposed Construction	AUO Proposed Construction	Phenix Proposed Construction
Indefinite under 35 U.S.C. § 112. To the extent the court finds that the term is not indefinite: “a stand-alone, non-volatile device that is electrically reprogrammable, the device including a programming interface and two gamma reference controllers physically connected to the programming interface, the two gamma reference controllers being physically connected to source drivers connected to a panel.”	Indefinite. Alternatively, to the extent the Court decides the term is not indefinite, the term should be construed as: Function: programming and storing gamma reference voltage values in storage cells that are used to generate gamma reference voltage outputs and switching between different gamma settings to implement dynamic gamma correction Structure: Fig. 2 (programming interface 230, gamma reference	No construction necessary; plain and ordinary meaning

	<p>controller 210, and gamma reference controller 220) AND Fig. 3 (programming engine 310, Analog Input, R/W, MUX 320, A0, A1, A2, and floating gate memory cells 330-337) AND Fig. 5 (Tdamp)</p> <p>OR</p> <p>Fig. 6 (programming interface, Vpp, MUX, A0, A1, Bank Select, B0, B1, B2, floating gate memory cells) AND Fig. 5 (Tdamp)</p> <p>and equivalents thereof</p>	
--	--	--

92. It is my opinion that the term “gamma reference control capability,” as used in Claim 1 of U.S. Patent No. 7,557,788 (the ‘788 Patent), is indefinite. This is because, whether analyzed under 35 U.S.C. § 112(f) as a means-plus-function limitation or otherwise, the patent does not provide a POSA with a clear understanding of its scope or the structure that performs its claimed functions.

93. The term “gamma reference control capability” appears in Claim 1, step (a) of the ‘788 Patent, which recites: “providing said display with gamma reference control capability which is electrically reprogrammable and non-volatile.” (‘788 Patent, 7:27-29). A person of ordinary skill in the art (POSA) would observe that the word *capability* in this context is a generic, placeholder term, suggesting an ability to perform functions without specifying the structure for doing so. The surrounding claim language, such as step (e) “Storing said gamma reference Voltage levels in said gamma reference control capability” (‘788 Patent, 7:41-42), describes functions. While the claim recites other elements like a “control circuit” (7:33) and “means for executing a predetermined algorithm” (7:35-36), it does not specify the physical structure for the “gamma reference control

capability” itself, which is primarily tasked with storing gamma reference voltages in an electrically reprogrammable and non-volatile manner.

94. I have been informed by Innolux’s counsel that under 35 U.S.C. § 112(f), claim language describing a function without reciting definite structure may be a “means-plus-function” limitation, and that legal precedent (e.g., *Williamson v. Citrix Online, LLC*) indicates that generic terms like “capability” coupled with functional language can trigger § 112(f) even without the word “means.” Counsel has further instructed me that for such limitations, the patent specification must disclose adequate corresponding structure (hardware or an algorithm) that performs the claimed function; otherwise, the limitation is indefinite.

95. The primary function of the “gamma reference control capability,” as per Claim 1 of the ‘788 Patent, is to provide an electrically reprogrammable and non-volatile way to store optimized gamma reference voltage levels (‘788 Patent, 7:27-29, 41-42).

96. Upon a thorough review of the ‘788 Patent, I find no disclosure of a specific structure, circuit, or algorithm that is identified as, or clearly corresponds to, the “gamma reference control capability” for performing this recited storage function. The specification and figures (e.g., ‘788 Patent Figs. 2, 3, 4A-B, 6) describe elements like a “Programming Interface,” “Gamma Reference Controller[s],” and “programmable analog floating gate memory cells” (see ‘788 Patent, 4:1-10, 2:61-3:29), but none are explicitly equated to the overall “gamma reference control capability” with its claimed functions. The prosecution history of the ‘788 Patent (e.g., Non-Final Office Action of July 22, 2008, and Applicant Response of October 22, 2008) also discusses the term functionally without pointing to specific corresponding structure.

97. A POSA would expect the patent to describe, with adequate specificity, what component or system constitutes this “capability” and how it achieves its functions. Without such disclosure, a POSA would be left to speculate. Thus, if “gamma reference control capability” is treated as a means-plus-function limitation, it is my opinion that it is indefinite for failure to disclose corresponding structure.

98. Even if the term “gamma reference control capability” is not analyzed under § 112(f), it is my opinion that it remains indefinite. Innolux’s counsel has informed me that patent claims must define the invention with reasonable certainty, such that a POSA can understand the scope of the claimed invention, a principle addressed in cases like *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898 (2014).

99. The term “gamma reference control capability” lacks the specificity for a POSA to determine its scope with reasonable certainty. The word “capability” is broad and does not denote a recognized class of structures in this technical context. The ‘788 Patent provides no objective boundaries or parameters (e.g., specific architecture, memory organization, interface details, or performance metrics) to clarify what structures fall within this term. A POSA could plausibly interpret it to refer to various elements or combinations shown in the patent, such as the “Programming Interface” (Fig. 2, element 230), the combined “Gamma Reference Controller[s]” (Fig. 2, elements 210, 220), or other implied systems, without clear guidance from the specification to resolve this ambiguity. Given this lack of clarity, a POSA would not be able to determine the precise scope of the term with reasonable certainty.

100. If, notwithstanding the indefiniteness concerns detailed above, the term “gamma reference control capability” is determined to be definite, a POSA looking to give it meaning would turn to the disclosed embodiments in the ‘788 Patent. In my opinion, the only way to provide

meaningful structural limitations to this term, based on the patent’s disclosure, is to tie it to the primary illustrated embodiment related to programming and storing gamma voltages. This involves the system depicted in Figure 2 of the ‘788 Patent and its accompanying description (2:61–3:29), specifically the “Programming Interface” (230) in conjunction with the two “Gamma Reference Controller[s]” (210, 220), which are described as being electrically reprogrammable and containing non-volatile memory. Thus, the only plausible alternative construction would be “a stand-alone, non-volatile device that is electrically reprogrammable, the device including a programming interface and two gamma reference controllers physically connected to the programming interface, the two gamma reference controllers being physically connected to source drivers connected to a panel.” This construction is the only one that appears to capture a tangible system from the specification that could arguably embody the claimed “capability” with the recited characteristics.

2. *Control circuit*

Innolux Proposed Construction	AUO Proposed Construction	Phenix Proposed Construction
<p>Indefinite under 35 U.S.C. § 112.</p> <p>To the extent the court determines that the term is not indefinite:</p> <p>a stand-alone integrated circuit attached to and separate from a liquid crystal display, the integrated circuit including a programming interface and two gamma reference controllers physically connected to the programming interface, the two gamma reference controllers being physically</p>	<p>Indefinite. Alternatively, to the extent the Court decides the term is not indefinite, the term should be construed as:</p> <p>Function: varying gamma reference voltage levels on columns of a display</p> <p>Structure: Fig. 2 (gamma reference controller 210 AND gamma reference controller 220) AND Fig. 3 (programming engine 310, Analog Input, R/W, MUX 320, A0, A1, A2, and drivers 340-347)</p>	<p>No construction necessary; plain and ordinary meaning</p>

connected to source drivers connected to a panel of the liquid crystal display.	OR Fig. 6 (programming interface, Vpp, MUX, A0, A1, Bank Select, B0, B1, B2, and drivers (not numbered))	
---	---	--

101. It is my opinion that the term “control circuit,” as used in Claim 1 of the ‘788 patent, is indefinite. This is because the patent does not provide a person of ordinary skill in the art (POSA) with a clear understanding of the structure or boundaries of this “control circuit” or how it performs its claimed function with reasonable certainty, whether analyzed under 35 U.S.C. § 112(f) as a means-plus-function limitation or under general definiteness principles.

102. The term “control circuit” appears in Claim 1, step (c) of the ‘788 Patent, which recites: “varying gamma reference Voltage levels on columns of said display by a control circuit, wherein said control circuit is separate from said display.” (‘788 Patent, 7:32-34). A POSA would observe that the term “circuit,” especially when preceded by a functional adjective like “control,” can be a generic structural term. When coupled with a function—here, “varying gamma reference Voltage levels on columns of said display”—it may invoke means-plus- function treatment.

103. I have been informed by Innolux’s counsel that under 35 U.S.C. § 112(f), claim language that recites a function without reciting sufficient definite structure for performing that function may be construed as a “means-plus- function” limitation. Counsel has further instructed me that for such limitations, the patent specification must disclose adequate corresponding structure (which could be hardware or an algorithm for software) that performs the claimed function; otherwise, the limitation is indefinite.

104. The function recited for the “control circuit” in Claim 1(c) is “varying gamma reference Voltage levels on columns of said display.” Upon a thorough review of the ‘788 Patent,

I find no disclosure of a specific, distinct structure or algorithm that is clearly identified as *the* “control circuit” for performing this particular “varying” function. The patents describe a “Programming Interface” (e.g., ‘788 Patent, Fig. 2, element 230) and “Gamma Reference Controller[s]” (e.g., ‘788 Patent, Fig. 2, elements 210, 220) which are involved in setting and outputting gamma voltages. The ‘788 Patent also describes a calibration process where “[a]utomating the testing of a panel can be achieved with optical sensors and feedback to the gamma correction section of the display. Once the optical sensors have modulated gamma reference Voltage levels for the columns... these values can be saved...” (‘788 Patent, 6:52-58). However, the specification does not delineate a specific “control circuit,” separate and distinct from other elements like the “means for executing a predetermined algorithm” (‘788 Patent, 7:38-39), that is clearly responsible for the act of “varying” the voltage levels on the columns as part of this calibration. The relationship between the “control circuit” and the “means for executing a predetermined algorithm” is not clarified; it’s uncertain if one is part of the other, or if they are entirely separate entities performing distinct sub-steps of the “varying” and “optimizing” process.

105. A POSA would expect the patent to describe, with adequate specificity, what component or system of components constitutes this “control circuit” and how it achieves the function of varying the voltage levels. Without such disclosure of a clearly linked structure performing this function, if “control circuit” is treated as a means-plus-function limitation, it is my opinion that it is indefinite.

106. Even if the term “control circuit” is not analyzed under § 112(f), it is my opinion that it remains indefinite. Innolux’s counsel has informed me that patent claims must define the invention with reasonable certainty, such that a POSA can understand the scope of the claimed invention.

107. The term “control circuit” is a generally understood term in electrical engineering, but in the context of Claim 1 of the ‘788 Patent, its specific metes and bounds are not reasonably certain. The patent does not provide a clear definition or description of what constitutes *this specific* “control circuit” that is “separate from said display” and performs the function of “varying gamma reference Voltage levels on columns.” A POSA would be left uncertain as to whether this “control circuit” refers to: 1. The on-chip programming interface of the gamma reference voltage generator ICs. 2. The gamma reference voltage generator ICs themselves (e.g., the AG1818). 3. An external device (like a PC connected for testing and calibration, which might also embody the “means for executing a predetermined algorithm”). 4. Some combination of these, or specific sub-parts thereof.

108. The specification does not provide sufficient detail to distinguish among these plausible interpretations or to clearly delineate the boundaries of the “control circuit” from other active components in the claimed calibration method, especially given that both the “control circuit” and the “means for executing a predetermined algorithm” are described as “separate from said display.” This lack of clarity would prevent a POSA from determining the scope of the term “control circuit” with reasonable certainty.

109. If, notwithstanding the indefiniteness concerns detailed above, the term “control circuit” is determined to be definite, a POSA seeking to understand its meaning within the context of the ‘788 Patent would look to the disclosed embodiments for a structural basis. The claim requires this “control circuit” to be “separate from said display” and to be capable of “varying gamma reference Voltage levels on columns of said display.” The most prominent, and indeed only, detailed structural embodiment in the ‘788 Patent that could perform such a function while being separate from the display panel itself is the gamma reference generator integrated circuit

system. Thus, to the extent the term is not indefinite, it should be construed as “a stand-alone integrated circuit attached to and separate from a liquid crystal display, the integrated circuit including a programming interface and two gamma reference controllers physically connected to the programming interface, the two gamma reference controllers being physically connected to source drivers connected to a panel of the liquid crystal display.” For example, Figure 2 of the ‘788 Patent depicts gamma reference controllers (210, 220) and a programming interface (230) as a system that is distinct from the TFT Panel (280). This integrated circuit system is described as being programmable to output a set of gamma correction reference voltages (‘788 Patent, Abstract; Fig. 6 illustrating the AG1818 programmable gamma reference generator). The programming interface allows the buffer outputs (the gamma voltages) to be set to desired values, which inherently includes the capability to *vary* these voltage levels during a calibration or programming process. Therefore, to give the term “control circuit” a definite structural meaning consistent with the patent’s disclosure, a POSA would reasonably understand it to refer to this stand-alone, programmable integrated circuit system. This system includes the programming interface and the gamma reference controllers which are, in turn, connected to the source drivers that drive the columns of the display. This interpretation anchors the “control circuit” in the main disclosed hardware system (e.g., the AG1818 IC) that enables the adjustment and provision of gamma reference voltages to the display, thereby performing the claimed function of varying those levels while being separate from the display.

3. *Means for executing a predetermined algorithm*

Innolux Proposed Construction	AUO Proposed Construction	Phenix Proposed Construction
The “means for executing” is a general purpose	(construing the term “means for executing a predetermined algorithm according to a predetermined criteria and data sensed by said at	Function: executing a predetermined algorithm

<p>processor. The term “predetermined algorithm” is Term 11 and is indefinite for the reasons stated as to Term 11.</p> <p>If the term is a Means-Plus-Function term, it is indefinite for failure to clearly define the claimed function, and for lack of corresponding structure or algorithm in the specification.</p>	<p>least one sensor / means for executing said predetermined algorithm”)</p> <p>Indefinite. Alternatively, to the extent the Court decides the term is not indefinite, the term should be construed as:</p> <p>Function: execution of an algorithm that optimizes gamma reference voltage levels based on (1) data sensed by at least one sensor and (2) the application that is being displayed, external environment such as temperature and ambient light, or the personal preference of the user</p> <p>Structure: Fig. 2 (programming interface 230), Ain, A0, A1, A2, R/W control signal</p> <p>or</p> <p>Fig. 6 (programming interface, Vpp, Aout, A0, A1), 6:1-14</p> <p>or</p> <p>6:57-64 (PC programming interface connected to monitors feeding back data from the display during optimization tuning at a time of manufacturing) and equivalents thereof</p>	<p>Structure: programming interface</p>
---	--	---

110. It is my opinion that the term “means for executing a predetermined algorithm,” as used in Claim 1 of the ‘788 Patent, could be understood by a person of ordinary skill in the art (POSA) to refer to a general-purpose processor programmed to perform the stated function. While the use of “means for” typically invokes 35 U.S.C. § 112(f), in this instance, the presumption is overcome because the recited function is one that a POSA would readily associate with a general-purpose processor, and the specification does not disclose a specific, novel structure for this purpose. Furthermore, an attempt to construe this term as a means-plus-function limitation tied to an insufficient or incorrect structure, such as the disclosed “programming interface,” is technically unsound.

111. I have been informed by Innolux’s counsel that the phrase “means for” followed by functional language generally creates a presumption that 35 U.S.C. § 112(f) (means-plus-function claiming) applies. However, counsel has also advised that this presumption can be overcome if the claim term, read in light of the specification, recites structure capable of performing the identified function, or if it recites a function that can be performed by a well-understood class of structures, such as a general-purpose computer or processor.

112. In this case, the function recited is “executing a predetermined algorithm.” A POSA would understand that executing algorithms, particularly for tasks like display calibration or optimization as suggested by the overall context of the ‘788 Patent (e.g., ‘788 Patent, 6:44-64, discussing PC-based optimization and automated testing with sensors), is a standard capability of a general-purpose processor or microcontroller. The ‘788 Patent itself provides support for this understanding when it mentions: “A PC based programming interface is available for prototyping and gamma optimization. ... Display optimization algorithms may be located in Such a PC...” (‘788 Patent, 6:44-49). This passage clearly indicates that the patentees envisioned the execution of such algorithms as occurring on a computer, which is fundamentally driven by a general-purpose processor. The specification of the ‘788 Patent does not describe any novel, specific hardware circuit or special-purpose logic uniquely designed for “executing a predetermined algorithm.” Instead, the functions and systems described are consistent with tasks performed by standard computational hardware. Therefore, a POSA reviewing this term would not look for a specialized, patent-specific structure but would understand it to refer to a general-purpose processor programmed to carry out the (unspecified) “predetermined algorithm.” The claim further requires this “means” to be “separate from said display” (‘788 Patent, 7:38-39), which is entirely

consistent with an external PC or a separate processing unit containing such a general-purpose processor.

113. If the term is thus not considered a § 112(f) limitation, it would be construed based on its plain and ordinary meaning to a POSA. In this context, that meaning would be a general-purpose processor capable of being programmed to execute an algorithm. Consequently, the specific indefiniteness concerns tied to lacking a *corresponding structure* under § 112(f) would not apply to this term, though the absence of a disclosed specific “predetermined algorithm” might raise separate definiteness questions under § 112(b) regarding the algorithm itself.

114. Hypothetically, if the term “means for executing a predetermined algorithm” were to be construed under § 112(f), it would, in my opinion, be indefinite. Innolux’s counsel has informed me that for a means-plus-function limitation to be definite, the specification must disclose adequate corresponding structure that performs the claimed function, and for computer-implemented functions, this typically requires disclosure of the algorithm itself.

115. The ‘788 Patent does not meet these requirements. Firstly, while the patent refers to a “predetermined algorithm” (‘788 Patent, 7:35), it never actually discloses the steps or logic of this algorithm. Without knowing the specific algorithm, a POSA cannot identify or build a specific structure (if a special-purpose one were intended) or configure a general-purpose one in the particular way that corresponds to that algorithm. Secondly, the specification does not link the function of “executing a predetermined algorithm” to any specific hardware component or disclosed software routine within the described gamma reference generator system itself that would perform this execution. As noted, the most direct reference to algorithm execution in the patent points to an external PC (‘788 Patent, 6:44-49). Therefore, if subjected to § 112(f), the term

would be indefinite due to the lack of a disclosed specific algorithm and the absence of a clearly linked corresponding structure within the patent for performing the execution of such an algorithm.

116. I understand that Phenix might argue that the “programming interface” disclosed in the patents constitutes the corresponding structure for the “means for executing a predetermined algorithm.” This position is, in my opinion, technically flawed because the disclosed “programming interface” lacks the necessary computational capability and serves a different purpose.

117. The ‘788 Patent describes the “Programming Interface” (e.g., ‘788 Patent, 6:1-14, Fig. 2, element 230) as primarily a set of connections and, at most, basic selection logic. For instance, the ‘788 Patent describes the “Programming Interface 230 comprises a common Analog Input (A) ... three address inputs (A0, A1, and A2) ... and a R/W control signal...” (‘788 Patent, 3:6-10). Other descriptions detail a Vpp input for programming voltage and mode selection, address inputs (A0, A1), and bank inputs (B0, B1, B2) used to select memory locations (‘788 Patent, 6:1-14, Fig. 4A, Fig. 6). A POSA would understand these descriptions and figures as depicting an interface for routing signals, selecting memory cells, and enabling read/write operations—essentially, a conduit for data and control signals, not a computational engine.

118. The function of “executing an algorithm” fundamentally requires processing capabilities, such as performing arithmetic operations, logical comparisons, conditional branching, and managing data flow according to the steps of an algorithm. The disclosed programming interface, consisting of pins, multiplexers (e.g., ‘788 Patent, Fig. 3, element 320), and input lines, does not possess these computational capabilities. To the extent an algorithm is executed to control the programming of the gamma reference generator IC, the “programming interface” is the means by which an external entity—such as the PC mentioned in the specification or a dedicated

microcontroller (which would itself contain a processor)—communicates with the IC. The interface facilitates the application of programming signals or the retrieval of data as dictated by an algorithm executed elsewhere; it does not perform the decision-making or step-by-step processing that constitutes algorithm execution. The entity performing the execution would be the processor within that external PC or microcontroller, not the pins and basic logic gates forming the interface on the gamma chip. Thus, identifying the on-chip “programming interface” as the structure for “executing a predetermined algorithm” is technically incorrect as it conflates a communication pathway with a computational unit.

4. *Predetermined Algorithm*

Innolux Proposed Construction	AUO Proposed Construction	Phenix Proposed Construction
Indefinite under § 112	<p>AUO’s and Indefinite. Alternatively, to the extent the Court decides the term is not indefinite, the term should be construed as:</p> <p>“an algorithm for optimizing gamma reference voltage levels for an LCD including following steps: [1] drive the R/W signal low or Vpp signal (and/or placing A0, A1, A2, B0, B1, B2 signals in 1, 1, 1, 1, 1, 1 configuration) high for said LCD; [2] selecting output or channel of an integrated circuit to program using A0-A2 and/or B0-B2 for said LCD; [3] determining a desired voltage for selected output using at least one optical sensor on said LCD, which provides data sensed for said LCD; [4] comparing optical data corresponding to an optimum gamma curve or predetermined criteria with the data sensed by said at least one sensor for said LCD; [5] based on a result of the foregoing comparison, determining if the predetermined criteria are met for each selected output/channel of said LCD; if so, continue to step [7] for said LCD; [6] in an event that the “predetermined criteria” are not met, varying gamma reference voltage levels and repeating Steps [3]-[5] for said LCD until the predetermined criteria are met for said LCD; [7] drive the R/W signal high or pulse the Vpp signal (and/or placing A0, A1, A2, B0, B1, B2 signals in 1, 1, 1, 1, 1, 1 configuration) for said LCD, and write the value on the analog input into memory for the output/channel selected by A0-A2 and/or B0-B2 for said LCD.</p>	No construction necessary; plain and ordinary meaning

	<p>OR</p> <p>an algorithm for optimizing gamma reference voltage levels for an LCD, including following steps: [1] preloading the integrated circuit of said LCD with a default configuration, which is close to the historical values for the majority of displays for said LCD; [2] drive the R/W signal low or Vpp signal (and/or placing A0, A1, A2, B0, B1, B2 signals in 1, 1, 1, 1, 1, 1 configuration) high for said LCD; [3] determining which parameter needs to be changed during testing for said LCD; [4] testing said LCD using at least one sensor for said LCD; [5] comparing optical data corresponding to an optimum gamma curve or predetermined criteria with the data sensed by said at least one sensor for said LCD; [6] based on a result of the foregoing comparison, determining if the predetermined criteria are met for each selected output/channel of said LCD; if so, continue to step [8] for said LCD; [7] in an event that the “predetermined criteria” are not met for said LCD, varying gamma reference voltage levels and repeating Steps [4]-[6] for said LCD until the predetermined criteria are met for said LCD; [8] drive the R/W signal high or pulse the Vpp signal (and/or placing A0, A1, A2, B0, B1, B2 signals in 1, 1, 1, 1, 1, 1 configuration) of said LCD, and write the value on the analog input into memory for the output/channel selected by A0-A2 and/or B0-B2 for said LCD</p>	
--	---	--

119. It is my opinion that the term “predetermined algorithm,” as used in Claim 1 of the ‘788 patent, is indefinite under 35 U.S.C. § 112(b). This is because the patent specification wholly fails to disclose the steps or logic of the algorithm itself, leaving a person of ordinary skill in the art (POSA) unable to determine with reasonable certainty what specific process the claim requires or what limitations it imposes.

120. Claim 1 of the ‘788 Patent recites a method of calibrating a liquid crystal display. Step (d) of this claim requires “optimizing said gamma reference Voltage levels using means for executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor, wherein said means for executing said predetermined algorithm is separate from said display to achieve the desired gamma curve;” (‘788 Patent, 7:35-40). This “predetermined algorithm” is therefore central to the claimed method step of optimizing the

gamma levels; it ostensibly defines the specific process by which optimization occurs, using sensor data and certain “predetermined criteria” (which are also undefined) to achieve the desired result. However, a POSA reading the ‘788 Patent would find no description of the actual steps, logic, flowchart, pseudocode, or mathematical operations that constitute the claimed “predetermined algorithm.”

121. I have been informed by Innolux’s counsel that under 35 U.S.C. § 112(b) and the standard set forth by the Supreme Court in *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898 (2014), patent claims must inform those skilled in the art about the scope of the invention with reasonable certainty. Counsel has also advised me that where a claim limitation involves a process or function defined by an algorithm, particularly one implemented by computer or processor, failure to disclose that algorithm sufficiently can render the claim indefinite.

122. In this case, the specification’s failure to disclose the algorithm is clear. While the patent mentions the existence of such algorithms, stating, for example, that “[d]isplay optimization algorithms may be located in such a PC [connected to a programming interface]” (‘788 Patent, 6:48-49) and referring elsewhere to “operating means for executing one or more optimization criteria algorithms” (‘788 Patent, 8:10-12 in claim 3), it provides absolutely no detail on what these algorithms *are* or how they function. The patent does not specify how the sensor data and the undefined “predetermined criteria” are processed to achieve the gamma optimization. Optimizing a gamma curve based on sensor data and criteria is a complex task, not a self-evident process. A POSA would recognize that numerous different algorithms could potentially be used, involving various mathematical approaches (like curve fitting, iterative adjustments, or lookup table modifications) and different ways of interpreting sensor data or applying criteria. Without disclosure of the specific algorithm chosen and claimed by the patentee, a POSA has no way to

know which specific optimization method falls within the scope of the claim. This uncertainty is compounded by the fact that the algorithm is claimed to operate according to “predetermined criteria,” which are themselves never defined or explained in the patent. A POSA cannot understand the algorithm without knowing the criteria it is designed to satisfy.

123. Because the ‘788 Patent fails to disclose the actual “predetermined algorithm,” a POSA cannot determine the scope of Claim 1, step (d) with reasonable certainty. A POSA cannot know what specific optimization process is patented, making it impossible to determine whether any particular calibration method infringes the claim. The term “predetermined algorithm” is thus reduced to a mere placeholder for *any* algorithm that might perform the optimization function, lacking the required certainty.

124. It is my opinion that the term “predetermined algorithm” in Claim 1 of the ‘788 Patent is indefinite because the specification provides no disclosure of the algorithm’s steps or logic. This lack of disclosure prevents a POSA from understanding with reasonable certainty the scope of the claimed optimization step, thereby failing the definiteness requirement of 35 U.S.C. § 112(b).

5. *Optimizing said gamma reference voltage levels*

Innolux Proposed Construction	AUO Proposed Construction	Phenix Proposed Construction
Indefinite under § 112	(No construction proposed)	No construction necessary; plain and ordinary meaning

125. It is my opinion that the term “optimizing said gamma reference voltage levels,” as used in Claim 1 of the ‘788 patent, is indefinite under 35 U.S.C. § 112(b). The patent fails to define what constitutes “optimizing” in this context or provide any objective standard or endpoint for the

optimization process, leaving a person of ordinary skill in the art (POSA) unable to determine the scope of this limitation with reasonable certainty.

126. Claim 1 of the ‘788 Patent recites a method of calibrating a liquid crystal display. Step (d) requires: “optimizing said gamma reference Voltage levels using means for executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor, wherein said means for executing said predetermined algorithm is separate from said display to achieve the desired gamma curve;” (‘788 Patent, 7:35-40). The term “optimizing” implies achieving the best or most effective state for the gamma reference voltage levels relative to the desired gamma curve. However, the concept of “optimal” is subjective and context-dependent unless defined by objective criteria.

127. I have been informed by Innolux’s counsel that under 35 U.S.C. § 112(b), patent claims must inform those skilled in the art about the scope of the invention with reasonable certainty.

128. In this case, the ‘788 Patent specification provides no such definition or objective standard for determining when the gamma reference voltage levels are considered “optimized.” A POSA reading the patent would find several deficiencies. First, the patent uses the word “optimizing” or “optimization” (e.g., ‘788 Patent, 6:46, 6:48, 8:10, 8:18, 8:23) but never defines what constitutes an optimized state for the gamma levels in this context. It is unclear whether optimization means minimizing deviation from a target curve, achieving a certain perceptual uniformity, meeting a specific numerical tolerance, or some other benchmark. Second, the optimization process is explicitly tied to the execution of a “predetermined algorithm” according to “predetermined criteria.” As discussed previously regarding the term “predetermined algorithm,” neither the algorithm nor the criteria are disclosed in the patent. Without knowing the

specific algorithm or the criteria it aims to satisfy, a POSA cannot understand the goal or endpoint of the “optimizing” step, or in that matter whether or not the optimization can even be achieved. Third, the claim states the goal is “to achieve the desired gamma curve,” but the patent does not specify how close the match must be to be considered “optimized.” It fails to clarify whether any improvement constitutes optimization, or if a specific threshold of accuracy must be met. This lack of objective boundaries leaves a POSA unable to determine when the claimed step of “optimizing” begins or ends, or what level of performance is required. For example, the description of automated testing mentions achieving “predetermined light matching” (‘788 Patent, 6:55-56), but fails to define what constitutes a sufficient “match.” Consequently, a POSA cannot ascertain the scope of the claimed method step with reasonable certainty.

129. It is my opinion that the term “optimizing said gamma reference voltage levels” in Claim 1 of the ‘788 Patent is indefinite because the specification fails to provide any objective standard, definition, or endpoint for the optimization process. This deficiency is compounded by the reliance on an undisclosed “predetermined algorithm” and undefined “predetermined criteria.” As a result, a POSA cannot determine the scope of this claim limitation with reasonable certainty, rendering it indefinite under 35 U.S.C. § 112(b).

6. *Gamma reference voltage levels*

Innolux Proposed Construction	AUO Proposed Construction	Phenix Proposed Construction
An analog voltage(s) stored in an analog storage cell	An analog voltage(s) stored in an analog storage cell	No construction necessary; plain and ordinary meaning

130. A person of ordinary skill in the art (POSA) at the time of the invention of the ‘788 Patent, having reviewed the patent’s claims, specification, and prosecution history, along with relevant extrinsic evidence, would understand the term “gamma reference voltage levels” to mean

an actual analog voltage that is stored in an analog storage cell. This understanding is based on the collective weight of the intrinsic and extrinsic evidence.

131. The language of Claim 1 of the '788 Patent, when read by a POSA, indicates that “gamma reference voltage levels” are tangible, physical electrical potentials. Claim 1 recites “A method of calibrating a liquid crystal display...comprising the steps:” including “c. varying gamma reference voltage levels on columns of said display...; d. optimizing said gamma reference voltage levels...; and e. storing said gamma reference voltage levels in said gamma reference control capability.”

132. A POSA would understand the step of “varying gamma reference voltage levels on columns of said display” to refer to the physical adjustment of actual electrical potentials applied to the columns of the display hardware itself. This implies direct manipulation of an analog quantity on the display hardware itself. Similarly, “optimizing said gamma reference voltage levels” refers to the adjustment of these applied analog voltages to achieve a desired display characteristic. Crucially, the subsequent step of “storing said gamma reference voltage levels” would be understood by a POSA as storing the actual determined analog voltage values themselves. If these “levels” were merely digital representations, their storage would necessitate subsequent digital-to-analog conversion before they could be “varied on columns,” a step for which the patent provides no disclosure, instead emphasizing direct analog storage as detailed in the '788 specification.

133. This understanding is reinforced by dependent Claim 2, which refers to generating “at least one different set of gamma reference voltage levels” for “different ambient display conditions.” This points to distinct collections of actual, physical voltage values tailored for specific conditions, further underscoring their analog nature.

134. The specification of the ‘788 Patent consistently describes the storage and use of voltage values themselves, leading a POSA to understand “gamma reference voltage levels” as analog quantities.

135. The Abstract of the ‘788 Patent states that the invention is a “programmable buffer integrated circuit which can be programmed to output a set of gamma correction reference Voltages...” and, critically, “if power is removed, since the Voltage value is stored in non-volatile, programmable memory, the gamma correction is retained.” A POSA would interpret “Voltage value is stored” to mean that the analog magnitude of the voltage itself is the data being preserved. This is reiterated in the Summary of the Invention, which explains that “the Voltage value is stored in non-volatile, programmable memory” (‘788 Patent, 2:19-21). The consistent emphasis is on storing the value—an analog quantity—of the voltage.

136. Furthermore, the ‘788 specification explicitly details analog storage mechanisms. It repeatedly describes the memory elements as “programmable analog floating gate memory cells” (e.g., ‘788 Patent, 3:50-51) and “an analog storage cell” (‘788 Patent, 4:3-4). It further clarifies: “Each output is internally connected to an analog storage cell which can be written with analog values, for example, of 1024 step (10 Bit) resolution” (‘788 Patent, 4:3-5; see also 5:39-42 describing 1,024 “analog values”). A POSA would understand that if the fundamental storage cells are designed to hold “analog values,” then the “gamma reference voltage levels” stored in and output by such cells must themselves be analog voltages.

137. The specification also distinguishes the invention from “complex digital approaches to this ‘analog’ problem” of gamma correction, criticizing them as “quite expensive” (‘788 Patent, 2:3-8). This framing presents the patented invention as an analog solution. A POSA

would infer that the “gamma reference voltage levels” are integral to this analog solution, not digital data that would align with the criticized digital approaches.

138. Significantly, a POSA would expect that if “gamma reference voltage levels” were stored as digital data (e.g., binary codes), the specification would necessarily disclose a Digital-to-Analog Converter (DAC) to transform this digital data into the actual analog voltages required by the display columns or drivers. The ‘788 specification is devoid of any such disclosure of DACs in this context. Instead, it consistently describes direct buffering and output of stored analog values, reinforcing that the “gamma reference voltage levels” are inherently analog.

139. The drawings of the ‘788 Patent visually corroborate an analog architecture for storing and handling the “gamma reference voltage levels.”

140. Figure 3 of the ‘788 Patent, for instance, depicts “programmable analog floating gate memory cells” (e.g., elements 330-337) directly connected to driver elements (e.g., element 340). A POSA would recognize this direct architectural connection, without any intervening DACs, as characteristic of a system where analog voltage levels are stored within the cells and then directly buffered for output to become, or to directly influence, the gamma reference voltages applied to a display. The absence of any DAC in the signal path from storage to output in any figure is a strong indication that the stored “levels” are themselves analog voltages.

141. Arguments made by the Applicant during the prosecution of the ‘788 Patent further support the understanding that “gamma reference voltage levels” are analog voltages. A POSA reviewing the prosecution history, particularly the Applicant’s Remarks in the response dated October 22, 2008 (filed in response to a Non-Final Rejection; hereinafter “October 22 Remarks”), would find statements consistent with this interpretation.

142. In distinguishing the claimed invention from the prior art reference Liaw (U.S. Patent No. 6,593,934), the Applicant repeatedly referred to steps such as “varying gamma reference voltage levels on columns of said display” and then “storing said gamma reference voltage levels” (October 22 Remarks, p. 6, discussing Claim 1), or “applying one or more different gamma voltages to said liquid crystal display columns” and then “storing said applied gamma voltages in reprogrammable, nonvolatile cells” (October 22 Remarks, p. 8, discussing Claim 3). A POSA would understand this language to mean that the actual physical voltage quantities that were varied or applied are what is being stored, not a digital representation.

143. The Applicant also explicitly noted that Liaw disclosed an “automatic Gamma parameter correction system with a digital/analog converter (DAC)” (October 22 Remarks, p. 9). When arguing for patentability, the Applicant distinguished their method of directly storing “applied gamma voltages” from Liaw’s DAC-based approach. The Applicant did not suggest their own system involved storing digital representations that would then require a DAC for output. This distinction further leads a POSA to understand that the Applicant was describing a system where the analog voltages themselves are stored.

144. Furthermore, when discussing then-pending Claim 4 which recited a “high voltage programming means,” the Applicant argued against Liaw which “would not require a high voltage source for programming” (October 22 Remarks, p. 10). A POSA would know that the ‘788 Patent describes using high voltage pulses to program its *analog* memory cells to precise analog levels (‘788 Patent, 6:1-14). The Applicant’s arguments regarding high voltage programming for the “gamma voltages” in the ‘788 Patent claims would thus be understood by a POSA as referring to the storage of these voltages as analog quantities in the type of analog memory cells detailed in the ‘788 specification.

145. Throughout the October 22 Remarks, the Applicant does not describe the “gamma reference voltage levels” as being digital codes or requiring digital-to-analog conversion. The focus remains on the direct manipulation and storage of “voltages” or “voltage levels.” Therefore, a POSA would conclude that the arguments made during prosecution are consistent with and support the interpretation that “gamma reference voltage levels” refer to actual analog voltages.

146. Extrinsic evidence further confirms that a POSA would understand “gamma reference voltage levels” in the context of the ‘788 Patent to refer to analog quantities. Authoritative technical sources underscore the analog nature of “voltage level” in display gamma correction. For example, Charles Poynton’s *A Technical Introduction to Digital Video* (John Wiley & Sons 1996), a text a POSA might consult, explains gamma correction in terms of the relationship between a video signal (which is a voltage) and the displayed luminance. This relationship and the voltages that define it are inherently analog at the point of light emission or control in an LCD. While digital systems can process gamma information, the “gamma reference voltage levels” as claimed—being varied on columns and stored—are understood by a POSA as the actual analog electrical potentials.

I declare under penalty of perjury that the foregoing is true and correct to the best of my knowledge,
belief and understanding.

Dated: May 8, 2025

A handwritten signature in black ink, appearing to read "Paul Min", written over a horizontal line.

Paul S. Min, Ph.D.

St. Louis, Missouri

EXHIBIT A

Paul S. Min, Ph.D.
Washington University in Saint Louis
(Webpage : <https://engineering.wustl.edu/faculty/Paul-Min.html>)

psm@wustl.edu
+1 (314) 853-6200 (phone)

Campus Box 1223
Academy Building Room 218A
St. Louis, MO 63130

Education

<u>Year</u>	<u>College or University</u>	<u>Degree</u>
1987	The University of Michigan	Ph.D. in Electrical Engineering
1984	The University of Michigan	M.S. in Electrical Engineering
1982	The University of Michigan	B.S. in Electrical Engineering

Professional Experience

From: 1990
To: Present
Organization: Washington University, St. Louis

Summary:

2015 - Senior Professor - Department of Electrical Systems Engineering

2011 – 2014 Chair – Undergraduate Curriculum, Department of Electrical and Systems Engineering

2000 – 2002 Chair – Graduate Curriculum, Department of Electrical and Systems Engineering

2002 - 2014 Associate Professor - Department of Electrical and Systems Engineering

1997 - 2008 On leave from full-time duty at Washington University – as Presidents of MinMax Technologies and Erlang Technology.)

1996 - 2002 Associate Professor - Department of Electrical Engineering

1996 Promoted with Tenure

1990 - 1996 Assistant Professor - Department of Electrical Engineering

- Teaching Experience
- “Transmission System and Multiplexing,” Washington University, ESE 571
 - “Electrical Laboratory I,” Washington University, EE 250.
 - “Communication Theory,” Washington University, ESE 471.
 - “Reliability and Quality Control,” Washington University, ESE 405/505
 - “Signaling and Control of Communications Networks,” Washington University, ESE 572.
 - “Introduction to Electronic Circuits,” Washington University, ESE232
 - “Queueing Systems and Discrete Stochastic Processes,” Washington University, EE 536 / CS 567.
 - “Digital Computer,” Washington University, EE 260M / CS 260.
 - “Data Networks,” Washington University, EE 530.
 - “Electrical Circuit Analysis,” Washington University, ESE 230.
 - “Computer/Communications System Analysis I,” Washington University, EE 557/ CS 557.
 - “Computer/Communications System Analysis II,” Washington University, EE558 / CS 558.
 - “Digital Systems Laboratory,” Washington University, EE 455 / CS 455.

From: 1999
 To: 2008
 Organization: Erlang Technology, Inc., St. Louis, Missouri
 Title: Founder and President
 Summary: Up to 70 employees, \$40M in total capital raised from 5 VCs and 3 Corporations
 Received “Product of Year” Award from Analog Zone Magazine in 2004

From: 1997
 To: 1999
 Organization: MinMax Technologies, Inc., St. Louis, Missouri
 Title: Founder and President
 Summary: Fabless semiconductor company, designing high performance switching ASICs

From: September 1987
 To: August 1990
 Organization: Bellcore, New Jersey
 Title: Member of Technical Staff
 Summary: Member of New Network Architecture Development Group

From: 1983
 To: 1987

Organization: Department of Electrical Engineering, The University of Michigan
 Title: Graduate Instructor
 Summary: Instructor for senior level Electrical Engineering Laboratory Class. Received a Best "Best Graduate Instructor Award" from the Department of Electrical Engineering

Professional Affiliations, Achievements & Awards

- Technical Program Committee, COMCAS 2021, Tel Aviv, November 2021.
- Technical Program Committee, COMCAS 2019, Tel Aviv, November 2019.
- Technical Program Committee, COMCAS 2017, Tel Aviv, November 2017.
- Technical Program Committee, COMCAS 2015, Tel Aviv, October 2015.
- Past-Chair, Saint Louis Section of the Institute of Electrical and Electronics Engineers (IEEE), 2015.
- Member of Executive Committee, Saint Louis Section of the IEEE, 2010-2015.
- Chair, Saint Louis Section of the IEEE, 2014.
- Technical Program Committee, COMCAS 2013, Tel Aviv, October 2013.
- Vice Chair, Saint Louis Section of the IEEE, 2013
- Treasurer, Saint Louis Section of the IEEE, 2012.
- The Best Paper Award at MOBILITY 2011, October 2011, Barcelona, Spain.
- Counselor, Student Chapter of the Year, the Institute of Electrical and Electronics Engineers, 2011.
- Award of Appreciation, Saint Louis Section of the Institute of Electrical and Electronics Engineers, 2011, for contribution to various activities of the Saint Louis Section the Institute of Electrical and Electronics Engineers.
- Secretary, Saint Louis Section of the IEEE, 2010.
- Counselor, Student Chapter of the Year, the Institute of Electrical and Electronics Engineers, 2010.
- Wall Street Journal Businessmen of Year, 2003.
- American Men and Women of Science, listed in 1997.
- Member, Eta Kappa Nu (Honor Society for Electrical Engineers), inducted in 1992
- Outstanding Achievement Award, Bellcore, 1990.
- 18th ISATA Award of Technical Excellence, the best paper award at ISATA 1988.
- Rockwell Fellow, Rockwell International, 1985, 1986.
- Outstanding Graduate Student Award, the University of Michigan, 1985.
- Outstanding Teaching Award, the University of Michigan, 1984, 1986.
- Member of Honor's College, the University of Michigan, 1979, 1980.

- Honor's Convocation, the University of Michigan, 1979.
- Outstanding Freshman Award, the University of Michigan, 1979.
- Woodhaven Rotary Club Scholarship, Woodhaven Rotary Club, 1978.
- Second Place Winner, the State of Michigan Mathematics Prize Competition, 1977.
- International Program Committee, *IASTED International Conference on Communications, Internet and Information Technology (CIIT 2005)*, Cambridge, Massachusetts from October 31-November 2, 2005.
- International Program Committee, *IASTED International Conference on Communications 2003*, Scottsdale, Arizona, 2003.
- International Program Committee, *Wireless and Optical Communications 2003*, Banff, Canada, 2003.
- International Program Committee, Session Chair, *Wireless and Optical Communications 2002*, Banff, Canada, 2002.
- Invited participant, *NSF Workshop on Enhancing International Cooperation in CS/CE Research and Education*, Portland, 1997.
- Session Chair, *the 1993 Conference on Information Sciences and Systems*, Baltimore, March 1997.
- Member, Board of Editors, *Journal of Network and Systems Management*, 1996-1998.
- Program Committee, *International Symposium on Integrated Network Management*, San Diego, 1997.
- Guest Editor, *Journal of Network and Systems Management, Special Issue on Routing in Broadband Networks*, December 1995 and June 1996.
- Invited participant, *ARPA Workshop on Survivability of Large Scale Systems*, Washington D.C., 1996.
- Special Event Organizer, *International Symposium on Integrated Network Management*, Santa Barbara, 1995.
- Organizing Committee, *International Symposium on Integrated Network Management*, Santa Barbara, 1995.
- Local Arrangements Chair, *IEEE Information Theory Workshop on Information Theory Multiple Access and Queueing*, St. Louis, 1995.
- Chair, *Communications Chapter, St. Louis Section of the IEEE*, 1995.
- Participant, *IEEE Information Theory Workshop on Information Theory, Multiple Access and Queueing*, St. Louis, 1995.
- Participant, *ARPA/AFOSR Non-Linear Optics and Communication Workshop*, Denver, 1994.
- Participant, *CNRI Giga Bit Network Workshop*, Washington D.C., 1993.
- Participant, *IFIP/IEEE International Workshop on Distributed Systems*, New Jersey, 1993.
- Program Committee, *International Conference on Computer Communications and Networks*, San Diego, 1992.
- Session Chair, *ISMM International Conference*, New Orleans, 1990.
- Senior Member, *IEEE*.

- Member, *IEEE Committee on Network Operations and Management*.
- Member, *IEEE Committee on Computer Communications*.
- Registered Specialist, *Hong Kong Research Grant Council*.
- Reviewer, *IEEE Transactions on Communications*.
- Reviewer, *IEEE Transactions on Networking*.
- Reviewer, *IEEE Journal on Selected Areas in Communications*.
- Reviewer, *Journal of Network and Systems Management*.
- Reviewer, *Telecommunication Systems*.
- Reviewer, *Computers and Electrical Engineering*.
- Reviewer, *ETRI Journal*.
- Reviewer, *IEEE Transactions on Automatic Control*.
- Reviewer, *IEEE Communications*.
- Book Reviewer, *Prentice Hall*.
- Book Reviewer, *Morgan Kaufmann Publishers, Inc.*
- Book Reviewer, *Irwin Publishing Co.*

University Activities:

- Undergraduate Studies Committee, School of Engineering and Applied Science (2012 – Present)
- Faculty Advisor for IEEE Student Chapter (2009 – Present)
- Ambassador for McDonnell International Scholar Academy (2007 – 2013)
- Web Development Committee (2006 – 2008)
- University Judicial Board (1998 - 2000)
- Resource Generation Committee (1994 - 1995)
- Top 20 Committee (1992 - 1995)
- Telecommunications Committee, Chair (1991 - 1997)
- Library Planning Committee (1991 - 1992)
- Computer Engineering Committee (1990 - 1996)
- Communications Curriculum Committee (1990 - 1992)
- Resources Committee (1990 - 1992)

Patents

<u>Patent No.</u>	<u>Date</u>	<u>Title</u>
10,623,323	04/14/20	Network Devices and a Method for Signature Pattern Detection
10,284,476	05/07/19	Hierarchical Pattern Matching Devices and Methods

7,110,411	09/19/06	Method of and Apparatus for WFQ Scheduling Using a Plurality of Scheduling Queues to Provide Fairness, High Scalability, and Low Computational Complexity
7,106,738	09/12/06	Method of and Apparatus for High Speed Packet Switching Using Train Packet Queuing and Providing High Scalability
6,859,455	02/22/05	Method of and Apparatus for Building and Using Multi-Dimensional Index Trees for Multi-Dimensional Data Objects
6,614,789	09/02/03	Method of and Apparatus for Matching Strings of Different Lengths
6,359,885	3/19/02	Multi-Channel Packet Switching Apparatus Having Traffic Flow Controlling and Checking Functions
6,128,292	10/03/00	Packet Switching Apparatus with Multi-Channel and Multi-Cast Switching Functions and Packet Switching System Using the Same
5,788,161	12/13/98	Network Designer for Communication Networks
5,526,352	06/11/95	Integrable Low Complexity Multi-Channel Switch
5,440,549	08/08/95	Nonblocking Multi-Channel Switching with Multicasting Capability

Publications

- Yu, Qixiang, Luo, Z., and Min, P.S., “Intrusion Detection in Wireless Sensor Networks for Destructive Intruders.” Proceedings of the APSIPA 2015 conference. December 16-19, 2015.
- Hung, C.P., and Min, P.S., “Simple Web Application Framework.” Submitted for publication in the IEEE Transactions on Cloud Computing.
- Luo, Z., and Min, P.S., “Parallel Implementation of Energy-Based Target Localization Methods in Wireless Sensor Networks.” Proceeding of the 2014 IEEE SOUTHEASTCON.
- Yu, Q., Luo, Z., and Min, P.S., “Intrusion Detection in Wireless Sensor Networks for Destructive Intruder.” Proceeding of 2014 International Conference on Smart Computing (SMARTCOMP 2014).
- Luo, Z., and Min, P.S., “Survey of Target Localization Methods in Wireless Sensor Networks,” 19th IEEE International Conference on Networks (ICON 2013), Singapore, December 11-13, 2013.
- Hung, C.P., and Min, P.S., “Deriving and Visualizing the Lower Bounds of Information Gain for Prefetch Systems,” 19th IEEE International Conference On Networks (ICON 2013), Singapore, December 11-13, 2013.
- Hung, C.P., and Min, P.S., “Access LUT without CAM - Improved Pearson Hashing for Collision Reduction,” 19th IEEE International Conference On Networks (ICON 2013), Singapore, December 11-13, 2013.
- Luo, Z and Min, P.S., “Target Localization in Wireless Sensor Networks for Industrial Control with Selected Sensors.” International Journal of Distributed Sensor Networks, Volume 2013 (2013), Article ID 304631.
- Hung, C.P., and Min, P.S. “Performance Evaluation of Distributed Mobile Application Virtualization Services,” International Journal on Advances in Internet Technology, Vol. 5, no. 3&4, 2012, pp. 65-83.

- Hung, C.P. and Min, P.S., "Performance evaluation of distributed application virtualization services using the UMTS mobility model," MOBILITY 2011 The First International Conference on Mobile Services, Resources, and Users, 23-29 Oct. 2011.
- Hung, C.P. and Min, P.S., "Service Area Optimization For Application Virtualization Using UMTS Mobility Model," International Conference on Internet Computing, pp. 128-134, Las Vegas, July 18-21, 2011.
- Hung, C.P. and Min, P.S., "Application Virtualization Using UMTS Mobility Model," ICOMP'11, September, 2011.
- Hung, C.P. and Min, P.S., "Infrastructure Arrangement for Application Virtualization Service," the 9th International Information and Telecommunication Technologies Symposium, Vol.1, pp. 78-85, Rio de Janeiro, December 2010.
- Hung, C.P. and Min, P.S., "Probabilistic Approach to Network-Based Virtual Computing," the 9th International Information and Telecommunication Technologies Symposium, Vol.1, pp. 117-124, Rio de Janeiro, December 2010.
- Shiravi, A. and Min, P. S., "On the Latency Bound of Proportional Nested-DRR with Credit Adjusting," *2007 Workshop on High Performance Switching and Routing HPSR 2007*, July 2007.
- Shiravi, A. and Min, P. S., "LOOFA-PB: A Modified LOOFA Scheduler for Variable-Length Packet Switching." *2007 IEEE International Conference on Communications (ICC 2007)*, Glasgow, June 2007.
- Shiravi, A., Kim, Y. G., and Min, P. S., "Congestion Prediction of Self-Similar Network through Parameter Estimation," *Proceedings of 2006 IEEE/IFIP Network Operations & Management Symposium*, April 2006, Vancouver.
- Shiravi, A., Kim, Y. G., and Min, P. S., "Traffic Dispatching Algorithm in Three-Stage Switch," *Proceedings of 5th International Conference on Networking*, April 2006, Mauritius.
- Shiravi, A., Kim, Y. G., and Min, P. S., "Proportional Nested Deficit Round Robin with Credit Adjusting," *Proceedings of 2nd Int'l Conf. on Quality of Service in Heterogeneous Wired/Wireless Networks (QShine 2005)*, Orlando, August 2005.
- Shiravi, A., Kim, Y. G., and Min, P. S., "Proportional Nested Deficit Round Robin: Improving the Latency of Packet Scheduler with an O(1) Complexity," *Proceedings of International Workshop on Advanced Architectures and Algorithms for Internet Delivery and Applications (AAA-IDEA 2005)*, Orlando, June 2005
- Kim, Y. G., Shiravi, A., and Min, P. S., "Prediction-Based Routing through Least Cost Delay Constraint," *Proceedings of IEEE IPDPS 2004*, Santa Fe, April 2004.
- Kim, Y. G. and Min, P. S., "On the Prediction of Average Queuing Delay with Self-Similar Traffic," *Proceedings of IEEE GLOBECOM 2003*, San Francisco, December 2003.
- Hu, C., Saidi, H., Yan, P. Y., and Min, P.S., "A Protocol Independent Policier And Shaper Using Virtual Scheduling Algorithm," *Proceedings of ICCAS 2002*.

- Hu, C., Saidi, H., and Min, P.S., “DB_WFQ: An Efficient Fair Queueing Using Binary Counter,” *Proceeding of Coins 2002*.
- Yoon, U. and Min, P.S., “Performance Analysis of Radio Link Control Mechanism in W-CDMA System”, IEEE VTC’01 Fall, October 2001, New Jersey
- Akl, B., Hegde, M.V., Naraghi-Pour, M., and Min, P.S., “Multi-Cell CDMA Network Design,” *IEEE Transaction on Vehicular Technology*, Volume 50, No. 3, pp. 711-722, May 2001.
- Yoon, U., Park, S., Min, P.S., “Performance Analysis of Multiple Rejects ARQ at RLC (Radio Link Control) for Packet Data Service in W-CDMA System,” *IEEE Globecom*, November 2000, San Francisco.
- Yoon, U., Park, S., Min, P.S., “Performance Analysis of Multiple Rejects ARQ for RLC (Radio Link Control) in the Third Generation Wireless Communication,” *WCNC*, September 2000, Chicago.
- Yoon, U., Park, S., Min, P.S., “Network Architecture and Wireless Data Service Protocol based on Mobile IP toward the Third Generation Wireless Communication,” *3G Wireless*, June 2000, San Francisco, pp. 211-215
- R.G. Akl, M.V. Hegde, M. Naraghi-Pour, P.S. Min, “Multi-Cell CDMA Network Design,” *IEEE International Conference on Communications*, June 2000.
- R.G. Akl, M.V. Hegde, M. Naraghi-Pour, P.S. Min, “CDMA Network Design to Meet Non-uniform User Demand,” *International Teletraffic Congress*, March 2000.
- R.G. Akl, M.V. Hegde, M. Naraghi-Pour, P.S. Min, “CDMA Network Design,” *IEEE Transactions on Vehicular Technology*.
- R.G. Akl, M.V. Hegde, M. Naraghi-Pour, P.S. Min, “Cell Placement in a CDMA Network,” *IEEE Wireless Communications and Networking Conference*, September 1999, Volume 2, pp. 903-907.
- R.G. Akl, M.V. Hegde, P.S. Min, “Effects of Call Arrival Rate and Mobility on Network Throughput in Multi-Cell CDMA,” *IEEE International Conference on Communications*, June 1999, Volume 3, pp. 1763-1767.
- Hegde, M.V., Schmid, O.A., Saidi, H., and Min, P.S., “Real-Time Adaptive Bandwidth Allocation for High-Speed ATM Switches,” accepted, *International Conference on Communications*, June 1999.
- Akl, B.G., Hegde, M.V., and Min, P.S., “Effects of Mobility on Network Throughput in Multicell CDMA Networks,” accepted, *International Conference on Communications*, June 1999.
- Akl, B.G., Hegde, M.V., Min, P.S., and Naraghi-Pour, M., “Flexible Allocation of Capacity in Multi-Cell CDMA Networks,” accepted, *Vehicular Technology Conference*, June 1999.
- R.G. Akl, M.V. Hegde, M. Naraghi-Pour, P.S. Min, “Flexible Allocation of Capacity in Multi-Cell CDMA Networks,” *IEEE Vehicular Technology Conference*, May 1999, Volume 2, pp. 1643-1647.

- Oh, M.S., and Min, P.S., "Reliability Analysis for One-Turn and Deflection Crossbar Architectures and Distributed Fault Recovery Scheme," *Proceedings of GLOBECOM 97*, Phoenix, November 1997.
- Kim, K.B., Yan, P.Y., Kim, K.S., Schmid, O., and Min, P.S., "A Growable ATM Switch with Embedded Multi-Channel Multicasting Property," *Proceedings of GLOBECOM 97*, pp. 222-226, Phoenix, November 1997.
- Kim, K.B., Yan, P.Y., Kim, K.S., Schmid, O., and Min, P.S., "MASCON: A Single IC Solution to ATM Multi-Channel Switching with Embedded Multicasting," *Proceedings of ISS 97*, pp. 451-458, Toronto, September 1997.
- Maunder, A.S., and Min, P.S., "Investigation of Rate Control in Routing Policies for B-ISDN Networks," *Proceedings of the 15th International Teletraffic Congress*, Washington D.C., June 1997.
- Yan, P.Y., Kim, K.B., Kim, K.S., and Min, P.S., "A Large Scale ATM Switch System Using Multi-Channel Switching Paradigm," *Proceedings of ATM Workshop*, Lisbon, Portugal, May 1997.
- Yan, P.Y., Kim, K.S., Min, P.S., and Hegde, M.V., "Multi-Channel Deflection Crossbar (MCDL): A VLSI Optimized Architecture for Multi-Channel ATM Switching," *Proceedings of IEEE INFOCOM 97*, Kobe, Japan, April 1997.
- Maunder, A., Rayes, A., and Min, P.S., "Analysis and Rate Controlling Link: Leaky Bucket with Finite Servers," *Proceedings of the 1997 Conference on Information Sciences and Systems*, Baltimore, March 1997.
- Shin, S.W., Min, P.S., and Kim, J.H., "Real Time Traffic Management System at Korean Mobile Telecom," *Proceedings of 19th Annual Pacific Telecommunications Conference*, pp. 113-121, Honolulu, Hawaii, January 1997.
- Min, P.S., Hegde, M.V., Chandra, A., and Maunder, A.S., "Analysis of Banyan Based Copy Networks with Internal Buffering," *Journal of High Speed Networks*, Volume 5, No. 3, pp. 259-275 November 1996.
- Vargas, C., Hegde, M.V., Naraghi-Pour, M., and Min, P.S., "Shadow Prices for Least Loaded Routing and Aggregated Least Busy Alternate Routing," *IEEE Transactions on Networking*, Volume 4, No. 5, pp. 796-807, October 1996.
- Shin, S.W., Kwon, S.M., and Min, P.S., "Capacity Analysis of CDMA with Nonuniform Cell Loading and Sizes," *Proceedings of the 34th Annual Allerton Conference*, October 1996.
- Hegde, M.V., Min, P.S., and Sohraby, K., "Note from Guest Editors," *Journal of Network and Systems Management*, Volume 4, No. 2, pp. 101-102, June 1996.
- Rayes, A. and Min, P.S., "Application of Shadow Price in Capacity Expansion of State Dependent Routing," *Journal of Network Systems Management*, Volume 4, No. 1, pp. 71-93, March 1996.
- Min, P.S., "PCS Revolution in the United States," *Electronics News*, No. 2277, January 22, 1996. Translated and published in Korean.

- Hegde, M.V., Min, P.S., and Sohraby, K., "Guest Editorial," *Journal of Network and Systems Management*, Volume 3, No. 4, pp. 347-349, December 1995.
- Min, P.S., Hegde, M.V., Saidi, H., and Chandra, A., "Nonblocking Copy Networks in Multi-Channel Switching," *IEEE Transactions on Networking*, Volume 3, No. 6, pp. 857-871, December 1995.
- Rayes, A. and Min, P.S., "Capacity Expansion of Least Busy Alternate Routing with Shadow Price," *Proceedings of GLOBECOM 95*, Singapore, November 1995.
- Min, P.S., Hegde, M.V., Chandra, A., and Maunder, A., "Throughput and Delay for Copy Networks with Internal Buffers," *Proceedings of the 33rd Annual Allerton Conference*, October 1995.
- Min, P.S., Hegde, M.V., Saidi, H., and Chandra, A., "Fanout Splitting in Nonblocking Copy Networks with Shared Buffering," *Proceedings of the 33rd Annual Allerton Conference*, October 1995.
- Min, P.S., Hegde, M.V., and Rayes, A., "Estimation of Exogenous Traffic Based on Link Measurements in Circuit-Switched Networks," *IEEE Transactions on Communications*, Volume 43, No. 8, pp. 2381-2390, August 1995.
- Maunder, A., Rayes, A., and Min, P.S., "Analysis of Routing Policies in Broadband Networks." Invited paper. *Canadian Journal of Electrical and Computer Engineering*, Special Issue on Planning and Designing of Broadband Networks, Volume 20, No. 3, pp. 125-136, July 1995.
- Min, P.S., Hegde, M.V., Saidi, H., and Chandra, A., "Architecture and Performance of Nonblocking Copy Networks with Multi-Channel Switching," *Proceedings of APCC 95*, pp. 531-535, Osaka, Japan, June 1995.
- Saidi, H., Min, P.S., and Hegde, M.V., "A New Structural Property of Statistical Data Fork," *IEEE Transactions on Networking*, Volume 3, No. 3, pp. 289-298, June 1995.
- Min, P.S., Saidi, H., and Hegde, M.V., "A Nonblocking Architecture for Broadband Multi-Channel Switching," *IEEE Transactions on Networking*, Volume 3, No. 2, pp. 181-198, April 1995.
- Min, P.S., Hegde, M.V., Saidi, H., and Chandra, A., "Multi-Channel Copy Networks: Architecture, Performance Model, Fairness, and Cell Sequencing," *Proceedings of IEEE INFOCOM 95*, pp. 931-938, Boston, April 1995.
- Min, P.S., Hegde, M.V., and Chandra, A., "Analysis of Packet Movements in Internally Buffered Copy Networks," *Third ORSA Telecommunications Conference*, p. 141, Boca Raton, Florida, March 1995.
- Maunder, A. and Min, P.S., "Routing for Multi-Rate Traffic with Multiple Qualities of Service," *Proceedings of the Third International Conference on Computer Communications and Networks*, pp. 104-108, San Francisco, September 1994.
- Saidi, H. and Min, P.S., "Performance Benefits of Multi-Channel Switching," *Proceedings of the 32nd Annual Allerton Conference*, pp. 583-592, September 1994.
- Min, P.S., "Book Review: 'Telecommunications Network Management into the 21st Century'," *IEEE Communications*, Volume 32, No. 7, pp. 5-8, July 1994.

- Saidi, H., Min, P.S., and Hegde, M.V., "Guaranteed Cell Sequence in Nonblocking Multi-Channel Switching," *Proceedings of IEEE INFOCOM 94*, Toronto, pp. 1420-1427, June 1994.
- Min, P.S., Hegde, M.V., Saidi, H., and Chandra, A., "Shared Buffering in Nonblocking Copy Networks," *Proceedings of the 1994 IEEE International Symposium on Information Theory*, Norway, p. 406, June 1994.
- Min, P.S., Hegde, M.V., and Rayes, A., "Real Time Traffic Estimation in Circuit-Switched Networks," *Proceedings of the 14th International Teletraffic Congress*, France, pp. 1175-1184, June 1994.
- Hegde, M.V., Min, P.S., and Rayes, A., "State Dependent Routing: Traffic Dynamics and Performance Benefits," *Journal of Network and Systems Management*, Volume 2, No. 2, pp. 125-149, June 1994.
- Saidi, H., Min, P.S., and Hegde, M.V., "Control of Packet Flow in Statistical Data Forks," *Proceedings of the 1994 International Conference on Communications*, New Orleans, pp. 415-419, May 1994.
- Saidi, H., Min, P.S., and Hegde, M.V., "Nonblocking Multi-Channel Switching in ATM Networks," *Proceedings of the 1994 International Conference on Communications*, New Orleans, pp. 701-705, May 1994.
- Maunder, A. and Min, P.S., "Analysis and Development of Routing Schemes for Multi-Rate, Multi-Point Traffic," *Proceedings of the 1994 Conference on Information Sciences and Systems*, Princeton, pp. 1041-1046, March 1994.
- Min, P.S., Hegde, M.V., and Chandra A., "Internal Buffering in Banyan-Based Copy Networks," *Proceedings of the 1994 Conference on Information Sciences and Systems*, Princeton, pp. 209-214, March 1994.
- Rayes, A. and Min, P.S., "Capacity Expansion in State Dependent Routing Schemes," *Proceedings of the 1994 Conference on Information Sciences and Systems*, Princeton, pp. 237-241, March 1994.
- Vargas, C., Hegde, M.V., Naraghi-Pour, M., and Min, P.S., "Shadow Prices for State Dependent Routing," *Proceedings of the 1994 Conference on Information Sciences and Systems*, Princeton, pp. 243-248, March 1994.
- Saidi, H., Min, P.S., and Hegde, M.V., "Non-Blocking Multi-Channel Switching." Invited paper. *Proceedings of the 31st Annual Allerton Conference*, pp. 335-344, September 1993.
- Min, P.S., Hegde, M.V., and Rayes, A., "Model Based Estimation of Exogenous Traffic," *Proceedings of the 1993 Conference on Information Sciences and Systems*, Baltimore, pp. 126-131, March 1993.
- Hegde, M.V., Min, P.S., and Rayes, A., "Performance Analysis of State Dependent Routing," *Proceedings of the 1993 Conference on Information Sciences and Systems*, pp. 695-700, Baltimore, March 1993.
- Hegde, M.V. and Min, P.S., "Telephone Networks," Magill Survey of Science Applied Science, Salem Press, pp. 2624-2630, 1992.

- Saidi, H., Min, P.S., and Hegde, M.V., "Assignment of 2^k Trunk Groups in Multi-Channel Switches Using Generalized Binary Addresses," *Proceedings of the 30th Annual Allerton Conference*, pp. 652-661, September 1992.
- Hegde, M.V. and Min, P.S., "Performance Analysis of State Dependent Routing." Invited paper. *Second ORSA Telecommunications Conference*, Boca Raton, Florida, February 1992.
- Rizzoni, R. and Min, P.S., "Detection of Sensor Failures in Automotive Engines," *IEEE Transactions on Vehicular Technology*, Volume 40, No. 2, pp. 487-500, May 1991.
- Min, P.S. and Hegde, M.V., "End-to-End Planning Models for Optimal Evolution of Telecommunications Network," *Proceedings of IEEE INFOCOM 90*, San Francisco, pp. 200-206, June 1990.
- Min, P.S., "Validation of Controller Inputs in Electronically Controlled Engines." Invited paper. *Proceedings of the 1990 American Control Conference*, pp.2887-2890, San Diego, May 1990.
- Min, P.S. and Youn, C., "Generic Equipment Models (GEM) for Consistent Planning of Telecommunications Networks," *Proceedings of the 1990 ISMM International Conference*, New Orleans, pp. 190-194, March 1990.
- Min, P.S., "Robust Application of Beard-Jones Detection Filter," *Advances in Computing and Control*, Springer-Verlag, Volume 130, pp. 162-173, 1989.
- Min, P.S. and Ribbens, W.B., "A Vector Space Solution to Incipient Sensor Failure Detection," *IEEE Transactions on Vehicular Technology*, Volume 38, No.3, pp. 148-158, August 1989.
- Min, P.S., "Robust Application of Beard-Jones Detection Filter," *Proceedings of the 1989 American Control Conference*, Pittsburgh, pp. 859-864, June 1989.
- Rizzoni, G. and Min, P.S., "Real Time Detection Filters for the On-board Diagnosis of Incipient Failures," *Proceedings of the 1989 International Symposium on Allied Technology and Automation*, pp. 1445-1466, Paper No. 89131, Florence, Italy, June 1989.
- Min, P.S., "Diagnosis of On-Board Sensors in Internal Combustion (IC) Engines," *Proceedings of the 1989 American Control Conference*, Pittsburgh, pp. 1065-1070, June 1989.
- Min, P.S., "Detection of Incipient Sensor Failures in Internal Combustion Engines," *Proceedings of the 1988 International Symposium on Allied Technology and Automation*, Paper No. 88038, Florence, Italy, June 1988.

Testimony Provided or Expected to Provide as Expert Witness

Matter: Patent Infringement for Wireless Local Area Networks
 Law Firm: Quinn Emanuel Urquhard & Sullivan LLP

Case Name: Certain Audio Players and Components thereof (II). U.S.I.T.C. Inv. No. 337-TA-1330.
 Testifying Expert for Google Inc.
 Completed in June 2023.
 (Expert reports submitted and deposited.)

Matter: Patent Infringement for Wireless Communications
 Law Firm: Alston & Bird
 Case Name: Atlas Global Technologies LLC v. ASUSTek Computers Inc. USDC WD TX
 Civil Action No. 6:21-cv-820
 Testifying Expert for ASUSTek
 Completed in November 2023
 (Expert report submitted.)

Matter: Patent Infringement for Wireless Communications
 Law Firm: Perkins Coie
 Case Name: Bell Northern Research, LLC v. HMD AMERICA, INC. et al., Case No.: 1:22-cv-22706-SCOLA/GOODMAN (S.D. Fla.)
 Testifying Expert for HMD
 Completed in December 2023
 (Expert report submitted. Deposited.)

Matter: Patent Infringement for Wireless Communications
 Law Firm: LAW OFFICES S. J. CHRISTINE YANG
 Case Name: Atlas Global Technologies LLC v. ZyXEL Communications Corp. et al., U.S.D.C., W.D.T.X., Waco Div., Case No. 6:22-cv-00355 Atlas Global Technologies LLC v. D-Link Corp. U.S.D.C., W.D.T.X., Waco Div., Case No. 6:22-cv-00520
 Testifying Expert for ZyXel
 Retained in March 2023.
 (Expert report submitted.)

Matter: Patent Infringement for Wireless Communications
 Law Firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP
 Case Name: Bell Northern Research v. MeidaTek Inc.
 Testifying Expert for MediaTek Inc.
 Retained in August 2023.

Matter: Patent Infringement for Home Security System
 Law Firm: Foley and Lardner LLP
 Case Name: Alarm.com v. Vivint, Inc., AAA Arbitration Case. No. 01-22-0004-5525 and U.S.D.C. Case No. 2:23-cv-00004-JRG-RSP (E.D. Tex.),
 Testifying Expert for Vivint, Inc.
 Completed in 2023.

Matter: Patent Infringement for Wireless Communications and Electronics

Law Firm: Perkins Coie
Case Name: Bell Northern Research, LLC v. HMD AMERICA, INC. et al., Case No.: 1:22-cv-22706-SCOLA/GOODMAN (S.D. Fla.)
Testifying Expert for HMD
Completed in December 2023.

Matter: Patent Infringement for Network Switches
Law Firm: Charhon Callahan Robson & Garza, PLLC
Case Name: Sable Networks, Inc. and Sable IP, LLC v. CouldFlare, Inc. U.S.D.C. WD Tx
Case No. 6:21-cv-261
Testifying Expert for CloudFlare, Inc.
Completed in January 2024.
(Expert report submitted and deposed.)

Matter: Patent Infringement for Network Security
Law Firm: Fish and Richardson
Case Name: Finjan LLC v. Palo Alto Networks, Inc. – Case No. 4:14-cv-04908-PJH. USDC
ND CA, Oakland Division.
Testifying Expert for Finjan LLC.
Retained in September 2022.
(Expert report submitted and deposed.)

Matter: Patent Infringement for Network Management
Law Firm: Irell & Manella LLP
Case Name: SNMP Research, Inc. & SNMP Research International, Inc. v. Broadcom Inc.,
Brocade Communications Systems LLC, & Extreme Networks, Inc. U.S.D.C.
E.D. Tennessee at Knoxville Case No. 3:20-CV-451
Testifying Expert for SNMP Research.
Retained in May 2022.

Matter: Inter Parte Reexamination for Wireless Communications
Law Firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP
Case Name: Patent reexamination in front of the U.S.P.T.O.
Testifying Expert for MediaTek
Retained in March 2023.

Matter: Patent Infringement for Network Switching
Law Firm: Baker Botts
Case Name: Corrigent Corp. v. Arista Networks, Inc., Case No. 1:22-cv-00497-UNA. USDC
Delaware
Testifying Expert for Arista
Retained in October 2022.

Matter: Patent Infringement for Mobile Devices
Law Firm: Fish and Richardson
Case Name: GComm v. Samsung, U.S.D.C. ED. TX. Case No.:2:22-cv-0078-JRG

Testifying Expert for Samsung
Completed in January 2024.

Matter: Patent Infringement for Wireless Networks
Law Firm: McKool Smith
Case Name: Certain Mobile Telephones, Tablet Computers with Cellular Connectivity, and Smart Watches with Cellular Connectivity, Components Thereof, and Products Containing Same. U.S.I.T.C. Inv. No. 337-TA-1299
Testifying Expert for Ericsson
Completed in July 2022.
(Expert report submitted and deposed.)

Matter: Patent Infringement for Semiconductor Manufacturing
Law Firm: Kramer Levin
Case Name: Oasis Tooling, Inc. v. Siemens Indus. Software, Inc., 1:22-cv-151 (D. Del.), Oasis Tooling, Inc. v. GlobalFoundries U.S. Inc., 1:22-cv-312 (D. Del.)
Testifying Expert for Oasis Tooling
Retained in June 2022.
(Expert reports submitted.)

Matter: Patent Infringement for Optical Networks
Law Firm: Duane Morris
Case Name: NextGen Innovations, LLC v. Infinera Corporation. U.S.D.C. ED. TX (Marshall)
Case No. 2:22-cv-00306-JRG-RSP / IPR
Testifying Expert for Infinera
Retained in April 2023.

Matter: Patent Infringement for Wireless Devices
Law Firm: King and Spalding LLP
Case Name: Intellectual Ventures, et. al. v. General Motors Company and General Company Motors, LLC, Case No. 6:21-CV-1088 pending in the Western District of Texas, Waco Division
Testifying Expert for General Motors
Completed in January 2023.
(Expert report submitted.)

Matter: Patent Infringement for Wireless Devices
Law Firm: Sterne Kessler
Case Name: Neo Wireless LLC v. Volkswagen Group of America, Inc. and Volkswagen Group of America Chattanooga Operations, LLC and related matters
Testifying Expert for Volkswagen
Completed in September 2023.
(Expert report submitted and deposed. IPR declarations submitted)

Matter: Patent Infringement for Wireless Networks
Law Firm: Covington & Burling LLP

Case Name: XR Communications, LLC v. D-Link Systems, Inc., No. 8:17-cv-00596
(Consolidated) (C.D. Cal.)
Testifying Expert for Hewlett Packard Enterprise
Completed
(Expert report submitted and deposed.)

Matter: Patent Infringement for USB Charging System
Law Firm: Orrick, Herrington & Sutcliffe LLP
Case Name: Fundamental Innovation Systems International LLC v. TCT Mobile (US), TCT
Mobile (US) Holdings, Inc., et al. U.S.D.C. Delaware No. 20-552-RGA-CJB
Testifying Expert for TCL
Completed in June 2022.
(Expert report submitted and deposed.)

Matter: Inter Parte Reexamination for Wireless Communications
Law Firm: Alston & Bird
Case Name: Patent reexamination in front of the U.S.P.T.O.
Testifying Expert for Nokia
Retained in May 2022.
(Expert report submitted.)

Matter: Patent Infringement for Network Management System
Law Firm: Morgan, Lewis & Bockius, LLP
Case Name: Certain Routers, Access Points, Controllers, Network Management Devices,
Other Networking Products, and Hardware and Software Components Thereof,
U.S.I.T.C. Inv. No. 337-TA-1227
Testifying Expert for Hewlett Packard, Netgear, and CommScope
Completed in August 2021.
(Expert report submitted, deposed, and testified during trial.)

Matter: Contract Dispute
Law Firm: Orrick, Herrington & Sutcliffe LLP
Case Name: Allied Telesis, Inc., et al vs. Micron Technology, Inc., Santa Clara County
Case No: 2015-1-CV-282977
Testifying Expert for Micron
Retained in 2021. Deposed in October 2021.
Completed in 2022

Matter: Patent Infringement for Security Systems
Law Firm: Forley and Lardner LLP
Case Name: Certain Residential Premises Security Monitoring and Automation Control
Panels, and Components Thereof (ITC Inv. No. 337-TA-1273) and ADT LLC et
al v. Vivint, Inc., Case No. 6:21-cv-00687 (W.D. Tex.)
Testifying Expert for Vivint, Inc.
Completed in April 2022.
(Expert report submitted, deposed, and testified during trial.)

Matter: Inter Parte Reexamination for Internet Communications

Law Firm: Perkins Coie

Case Name: Patent reexamination in front of the U.S.P.T.O.
Testifying Expert for Twitter
Retained in June 2020.
(Expert report submitted.)

Law Firm: Fisher Broyles

Case Name: Vaxcel International Co., Ltd. v. Heathco LLC, U.S.D.C. Delaware No. 20-224-LPS
Testifying Expert for Vaxcel
Retained in February 2021.
(Expert report submitted and deposed.)

Matter: Patent Infringement for Network Communication System

Law Firm: Charhon Callahan Robson & Garza, PLLC

Case Name: Sable Networks, Inc. and Sable IP, LLC, v. ClouFlare, Inc. U.S.D.C. WDTX,
Civil Action No. 6:21-cv-261
Testifying Expert for CloudFlare, Inc.,
Completed in January 2024.

Matter: Patent Infringement for Mobile Wireless Device

Law Firm: Pearl Cohen

Case Name: In the Matter Of Certain UMTS And LTE Cellular Communications Modules
And Products Containing The Same, U.S.I.T.C. Inv. No. 337-TA-1240
Testifying Expert for Telit Wireless Communication, Quectel, and Thales
Completed in March 2023.
(Expert reports submitted and deposed.)

Matter: Transactional Taxes for Internet Application

Law Firm: Ryan Rapp & Underwood, PLC

Case Name: ADP, LLC v. Arizona Department of Revenue (TX2018-000246),
Testifying Expert for ADP, LLC.
Completed in June 2020.
(Expert report submitted.)

Matter: Trade Secret Misappropriation in Digital Electronics

Law Firm: Goodwin Proctor LLP

Case Name: Guzik Technical Enterprises versus Keysight Technologies, Inc. Superior Court
of the State of California for the County of Santa Clara, Case No.: 19CV355879
Testifying Expert for Keysight Technologies, Inc.
Retained in August 2020.

Matter: Patent Infringement for Fiber Optic Devices

Law Firm: Cooley

Case Name: Certain High-Density Fiber Optic Equipment and Components Thereof,
U.S.I.T.C. Inv. No. 337-TA-1194
Testifying Expert for AFL Communications, Panduit, FS.Com, Wirewerk, and
Siemon
Completed in October 2020.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Optical Transport Networks
Law Firm: Venerble
Case Name: Huawei Technologies Co. Ltd v Verizon Communications, Inc., et. al., 2:20-cv-
0030
Testifying Expert for Verizon.
Retained in March 2020.
(IPR declarations submitted.)

Matter: Patent Infringement for Lighting System
Law Firm: Fisher Broyles
Case Name: Vaxcel International Co., Ltd., v. Jasco Products Company, LLC., (Case No.
USDC Western District of Oklahoma, 5:19-CV-00154-JD
Testifying Expert for Vaxcel.
Retained in August 2020.

Matter: Patent Infringement for Wireless Communication
Law Firm: McDermott Will & Emery
Case Name: Bell Northern Research LLC v. ZTE. (Case No. 3:18-cv-01786 - S.D. Cal)
Testifying Expert for ZTE.
Retained in July 2019.
(IPR declarations submitted.)

Matter: Patent Infringement for Wireless Communication
Law Firm: Jones Day
Case Name: Bell Northern Research LLC v. Kyocera Corp. (Case No. 3:18-cv-1785 - S.D.
Cal)
Testifying Expert for Kyocera.
Completed in May 2019.
(Claim construction declaration submitted, and deposed.)

Matter: Patent Infringement for Electronic Payment Systems
Law Firm: Paul Hastings
Case Name: ID Tech Corp. v. Samsung Electronics Co., Ltd., et al. (Case No. No. 8:17-cv-1748-
DOC-JDE (C.D. Cal))
Testifying Expert for Samsung.
Retained in January 2019.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Internet Switching

Law Firm: Maynard Cooper
Case Name: Parity Networks, LLC v. Juniper Networks, Inc., Case No. 6:17-CV-00495-RWS-KNM (U.S.D.C.E.D. Tx.)
Testifying Expert for Juniper.
Retained in April 2018.
(IPR declarations submitted.)

Matter: Patent Infringement for Internet Switching
Law Firm: Morgan Lewis
Case Name: Parity Networks, LLC v. Hewlett Packard Enterprise Company, Case No. 6:17-CV-00682 (U.S.D.C.E.D. Tx.)
Testifying Expert for Hewlett Packard Enterprise Company.
Retained in September 2018.
(IPR declarations submitted.)

Matter: Inter Parte Rexamination for Covered Business Method
Law Firm: Reed Smith LLP
Case Name: NASDAQ v. Miami International
Expert for Miami International.
Retained in February 2018.
(Expert declarations submitted, and deposited.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Quinn Emanuel
Case Name: Qualcomm v. Apple, Case No. 3:17-cv-00108-GPC-MDD (U.S.D.C.S.D. Cal.)
Testifying Expert for Qualcomm.
Completed in April 2019.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Communication Devices
Law Firm: Venable
Case Name: Sycamore IP Holdings LLC v. Verizon Communications Inc, Case No. 2:16-cv-591-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for Verizon and Level 3.
Completed in September 2017.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Alston Bird
Case Name: Huawei Technologies Co. Ltd. V. Nokia Solutions and Networks, Case No. 2:16-cv-0056-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for Nokia.
Completed in December 2017.
(Expert reports submitted.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Quinn Emanuel
Case Name: Huawei Technologies Co. Ltd. V. Samsung Electronics C. Ltd, Case No. 3:16-cv-02787 (U.S.D.C. N.D. Cal)
Testifying Expert for Samsung.
Completed in March 2019.
(Expert reports submitted, and deposed.)

Matter: Arbitration for Licensing
Law Firm: Alston Bird
Case Name: Nokia v. LG Electronics, International Chamber of Commerce Arb. No. 21326
Testifying Expert for Nokia.
Completed in October 2016.
(Expert reports submitted.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Ropes and Gray
Case Name: Godo Kaisha IP Bridge 1 v. TCL Communication Technology Holdings, Case No. 15-634-SLR-SRF (U.S.D.C.S.D. Delaware.)
Testifying Expert for IP Bridge.
Completed in October 2018.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Paul Hastings
Case Name: Odyssey Wireless, Inc., v. Samsung Electronics Co., Ltd., et al, Case No. 3:15-cv-1738-H-RBB (U.S.D.C.S.D. Cal.)
Testifying Expert for Samsung.
Completed in October 2016.
(Expert reports submitted.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Greenberg Traurig
Case Name: Mobile Telecommunications Technologies LLC v. Amazon.com, Inc., 2:13-cv-883-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for Amazon.
Completed in April 2015.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Mayer Brown
Case Name: Mobile Telecommunications Technologies LLC v. LG Electronics Mobilecomm U.S.A., Inc., 2:13-cv-947-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for LG Electronics Mobilecomm.
Completed in February 2016.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Semiconductor Devices
Law Firm: Mayer Brown
Case Name: Inter Parte Reexamination for U.S. Patent Nos. 6,895,520 and 6,899,332
Expert for LG Electronics.
Completed in February 2016.
(Expert declaration submitted, and deposited.)

Matter: Patent Infringement in Vehicular Electronics
Law Firm: Gardner, Linn, Burkhardt & Flory, L.L.P
Case Name: *Magna Electronics Inc. v. TRW Automotive Holdings Corp. et al.*, Civil Action
No. 1:12-cv-00654 (Western District of Michigan), and relating to the action
styled *Magna Electronics Inc. v. TRW Automotive Holdings Corp. et al.*, Civil
Action No. 1:13-cv-00324 (Western District of Michigan).
Testifying Expert for Magna Electronics
Completed in February 2016.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement in Electronic Circuits
Law Firm: Ropes and Gray
Case Name: Certain Devices Containing Non-Volatile Memory and Products Containing the
Same (USITC Inv. Nos. 337-TA-922)
Testifying Expert for Spansion Inc.
Completed in February 2015.
(Expert reports submitted.)

Matter: Trade Secret Misappropriation in Software Method for Cable Television
Advertisement
Law Firm: Brownstein Hyatt Farber Schreck
Case Name: Cross MediaWorks v. EMT Holdings, USDC Southern District of New York,
Case No. 1:14-cv-00561-VSB
Testifying Expert for Cross MediaWorks.
Completed in April 2015.
(Testified during injunction hearing.)

Matter: Patent Infringement in Vehicular Electronics
Law Firm: Steptoe and Johnson
Case Name: Certain Vision-Based river Assistance System Cameras and Components Thereof
(USITC Inv. Nos. 337-TA-899 and 907)
Testifying Expert for Magna Electronics
Completed in February 2015.
(Expert reports submitted, deposited, and testified during trial.)

Matter: Patent Infringement for Vehicular System
Law Firm: Susman Godfrey

Case Name: Eagle Harbor Holdings, LLC, and Mediustech, LLC, v. Ford Motor Company, 3:11-cv-05503-BHS (U.S.D.C. Western District of Washington at Tacoma)
Testifying Expert for Mediustech.
Completed in March 2015.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Communication Networks
Law Firm: Davis Polk & Wardwell LLP
Case Name: Sprint Communications Company L.P., v. Comcast Cable Communications, LLC, Comcast IP Phone, LLC, and Comcast Phone of Kansas, LLC. 2:11-cv-02684-KHV-DJW (U.S.D.C. Kansas)
Testifying Expert for Comcast.
Retained in March 2012.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Communication Networks
Law Firm: Quinn Emanuel
Case Name: France Telecom S.A. v. Marvell Semiconductor, Inc., 12-Civ-4986 (S.D.N.Y.)
Testifying Expert for Marvell.
Completed in September 2014.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Wireless Image Distribution
Law Firm: Jones Day
Case Name: *Inter Partes* Review of U.S. Patent No. 8,437,797
Expert for Google Inc.
Completed in November 2014.
(Expert declaration submitted.)

Matter: Nonvolatile Semiconductor Memories
Law Firm: Jones Day
Case Name: *Inter Partes* Review of U.S. Patent Nos. 8,301,833 and 8,516,187
Expert for SanDisk.
Completed in May 2014.
(Expert declaration submitted.)

Matter: Communication Protocols for Wireless Device
Law Firm: Dorsey & Whitney, LLP
Case Name: Certain Point-To-Point Network Communication Devices and Products Containing Same (USITC Inv. No. 337-TA-892)
Testifying Expert for Toshiba
Completed in May 2014.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Wireless Networks
Law Firm: Ropes and Gray

Case Name: In the Matter of Certain Wireless Devices With 3G and/or 4G Capabilities and Components Thereof (USITC Inv. No. 337-TA-868) InterDigital Comms., Inc. v. Huawei Techs. Co., Ltd., No. 13-00008 (D. Del., filed January 2, 2013), InterDigital Comms., Inc. v. ZTE Corp., No. 13-00009 (D. Del., filed January 2, 2013), InterDigital Comms., Inc. v. Nokia Corp., No. 1:13-cv-00010 (D. Del., filed January 2, 2013), InterDigital Comms., Inc. v. Samsung Elec. Co., Ltd., No. 13-00011 (D. Del., filed January 2, 2013)
 Testifying Expert for Joint Defense Group.
 Completed in February 2014.
 (Expert reports submitted, deposed, and testified during trials.)

Matter: Patent Infringement for Mobile Communication
 Law Firm: Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.
 Case Name: Certain Digital Media Devices, Including Televisions, Blu-Ray Disc Players, Home Theater Systems, Tablets and Mobile Phones, Components Thereof and Associated Software (USITC Inv. No. 337-TA-882)
 Testifying Expert for LG Electronics, Inc.
 Completed in February 2014.
 (Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Wireless Networks
 Law Firm: Vinson & Elkins LLP
 Case Name: Wi-LAN USA, Inc. and Wi-LAN, Inc. v. Telefonaktiebolaget LM Ericsson and Ericsson, Inc. (USDC: Southern District of FL - Case #1: 12-cv-23569), Wi-LAN USA, Inc. and Wi-LAN, Inc. v. Alcatel-Lucent USA, Inc. (USDC: Southern District of FL - Case #1: 12-cv-23568-Altonaga/Simonton)
 Testifying Expert for Wi-LAN.
 Completed in May 2015.
 (Expert reports submitted, and deposed.)

Matter: Patent Infringement for Data Storage
 Law Firm: Ropes and Gray, Weil Gotshal
 Case Name: Summit Data Systems, LLC v. EMC Corporation., et al. 1:10-cv-00749-GMS (U.S.D.C. Delaware)
 Testifying Expert for EMC Corporation and Netapp, Inc.
 Completed in December 2012.
 (Expert reports submitted, and deposed.)

Matter: Patent Infringement for Wireless Mobile Device
 Law Firm: Ashurst Australia
 Case Name: Samsung v. Apple, Australian Federal Court Proceeding No. NSD 1243 of 2011
 Testifying Expert for Samsung Electronics.
 Completed in December 2012.
 (Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Wireless Mobile Devices

Law Firm: Quinn Emanuel
Case Name: Apple Inc. v. Samsung Electronics Co., Ltd., et al., 4:11-cv-01846-LHK (N.D. Cal.) and Samsung Electronics Co., Ltd., et al. v. Apple Inc., 4:11-cv-02079 (N.D. Cal.)
Testifying Expert for Samsung Electronics.
Completed in July 2012.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Wireless Mobile Device
Law Firm: Quinn Emanuel
Case Name: Certain Electronic Devices, Including Wireless Communication Devices, Portable Music And Data Processing Devices, And Tablet Computer, U.S.I.T.C. Inv. No. 337-TA-794
Testifying Expert for Samsung Electronics.
Completed in June 2012.
(Expert reports submitted, deposited, and testified during trial.)

Matter: Patent Infringement for Portable Storage Device
Law Firm: White and Case
Case Name: CERTAIN UNIVERSAL SERIAL BUS (“USB”) PORTABLE STORAGE DEVICES, INCLUDING USB FLASH DRIVES AND COMPONENTS THEREOF, US International Trade Commission Investigation No. 337-TA-788
Testifying Expert Witness for Trek
Completed in May 2012.
(Expert reports submitted, and deposited.)

Matter: Copyright Infringement for Petroleum Processing Software
Law Firm: Osha Liang LLP
Case Name: Aspen Technology, Inc. v. Tekin A. Kunt and M3 Technology, Inc., Case Number: H-10-1127, US District Court, Texas, Houston Division.
Testifying Expert for M3 Technology, Inc.
Completed in May 2012.
(Expert reports submitted, deposited, and testified during trial.)

Matter: Trade Secret Misappropriation for DC-DC converter
Law Firm: Covington & Burling, Haynes Boone
Case Name: Certain DC—DC Controllers and Products Containing Same, US International Trade Commission Investigation No. 337-TA-698
Testifying Expert for UPI.
Completed in March 2012.
(Expert reports submitted, deposited, and testified during trial.)

Matter: Patent Infringement for Parallel Processor
Law Firm: Orrick, Herrington, & Sutcliffe. Kirkland and Ellis.
Case Name: BIAx Corporation v. Nvidia and Sony Civil Action No. 09-cv-01257-PAB-MEH
Testifying Expert for Nvidia and Sony

Completed in March 2012.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Call Center Technology
Law Firms: Duffy, Sweeney, and Scott. Foley Lardner.
Case Name: Ronald Katz Technology Licensing v. Citizens Financial Group 7-ML-1816-C
RGK (FFM)
Testifying Expert Witness for Citizens Financial Group.
Completed in 2011.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Storage Area Network
Law Firm: DLA Piper
Case Name: Network Appliance, Inc., v. Sun Microsystems, Inc., Case Number: C-07-06053
EDL, US District Court, Northern District of California, San Francisco Division.
Testifying Expert for Sun Microsystems, Inc.
Completed in 2010.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Flat Panel Display Controller
Law Firm: Jones Day
Case Name: Certain Video Displays, Components Thereof, and Products Containing Same, US
International Trade Commission Investigation No. 337-TA-687
Testifying Expert for Vizio, Inc.
Completed in 2010.
(Expert reports submitted, deposited, and testified during trial.)

Matter: Patent Infringement for Call Center Technology
Law Firms: Foley Lardner
Case Name: Ronald Katz Technology Licensing v. US Bank 7-ML-1816-C RGK (FFM)
Testifying Expert Witness for US Bank
Completed in May 2009.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for USB to VGA Converter
Law Firm: Wang Hartmann, Gibbs, & Cauley, P.C.
Case Name: Displaylink Corporation v. Magic Control Technology Corporation, Case No.
5:07-CV-01998-RMW, US District Court, Northern District of California, San
Francisco Division.
Testifying Expert for Magic Control Technology Corporation
Completed in 2009.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Flash Memory
Law Firm: Jones Day and Wilson Sansini

Case Name: Certain Flash Memory Controllers, Drives, Memory Card, and Media Players and Products Containing Same. US International Trade Commission Investigation No. 337-TA-619

Testifying Expert for SanDisk Corporation.

Completed in 2008.

(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Semiconductor Packaging

Law Firm: Jones Day

Case Name: Certain Semiconductor Chips with Minimized Chip Package Size and Products Containing the Same. US International Trade Commission Investigation No. 337-TA-605

Testifying Expert for Freescale Semiconductor

Completed in 2008.

(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Automatic Switching System

Law Firms: Jones Day, and Heller Ehrman, LLP.

Case Name: ATEN International Co., Ltd and ATEN Technology, Inc. v. Belkin Corporation, Belkin Logistics, Inc. and Emine Technology Co., Ltd. US International Trade Commission Investigation No. Ltd 337-TA-589

Testifying Expert for Belkin Corporation, Belkin Logistics, Inc., and Emine Technology Co., Ltd.

Completed in 2007.

(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Dual Mode Communication

Law Firm: Wilmer Cutler Pickering Hale and Dorr, LLP

Case Name: Broadcom Corporation v. Qualcomm Incorporated SACV05-467-JVS (RNBx) Testifying Expert Witness for Broadcom Corporation

Completed in 2007.

(Expert reports submitted, deposed, and testified during trial.)